

SECTION IV. THEORY OF OPERATION

14.4.1 INTRODUCTION

This section describes, at system level, the single-cabinet ASOS (SCA). Information on common subassemblies that are also used at multicabinet ASOS sites is provided in respective chapters of this STM. Each ASOS is configured to meet the specific requirements of a given site. To configure an SCA system, a site survey must first be made in which the following factors must be considered:

- ! If the site is at an airport, appropriately locate sensor groups by considering runway patterns and lengths
- ! Mapping areas of frequent meteorological discontinuity
- ! Locating backup sensor group(s) for optimum system reliability
- ! Identifying the most suitable location for the SCA
- ! Identifying required sensors
- ! Measuring distances from planned sensor group(s) to SCA and from SCA to the air traffic controller (ATC) or operations area
- ! Assessing commercial power availability and reliability
- ! Specifying the number and types of users that need to access system data and control system functions. (Typically, the maintenance technician will be the only local user at single-cabinet ASOS sites; however, some sites could have other local users. The technician can control and monitor the system from a laptop PC when the PC data cable is connected to SCA P19.)

NOTE

SCA is used herein as an acronym for the single-cabinet ASOS to distinguish the SCA cabinet from the standard ASOS ACU cabinet.

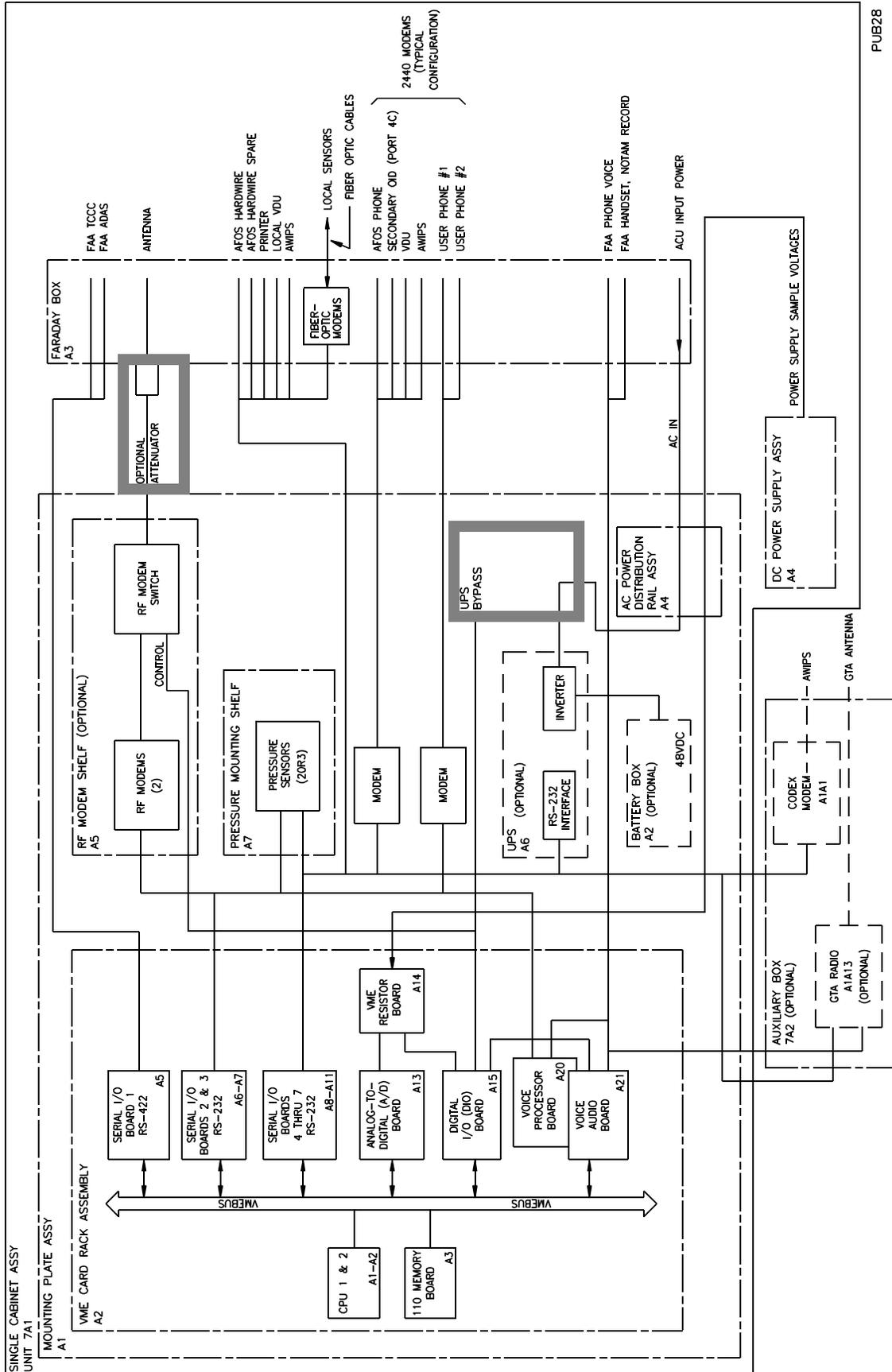
14.4.2 SCA BLOCK DIAGRAM

The typical SCA houses all equipment (except external sensors) required for stand-alone, automatic, surface weather data acquisition, reporting, and archiving. At Class II sites, an auxiliary box (aux box) is added when needed to house certain optional equipment. At Class I sites and reduced-capability sites, the aux box is an optional add-on.

As shown on the simplified block diagram (figure 14.4.1) the SCA receives sensor data, processes data in accordance with programmed instructions (algorithms) suitable for each sensor type, outputs data to peripheral devices and users, and archives data in internal memory. The SCA also contains a speech processor which digitizes English words that have been humanly vocalized and recorded. Digitized words (rather than phonemes, i.e., phonetic sounds, as in most synthesizers) are then syntactically assembled in accordance with current weather observation data to convey routine meteorological reports (METAR's), or special meteorological reports (SPECI's) for transmission over telephone lines or radio. The SCA mounts all data processing boards in 21-slot VME Rack 7A1A1A2.

NOTE

In the following paragraphs, reference designators for VME circuit card assemblies (CCA's) are abbreviated to identify only the CCA number within the VME rack.



PUB28

Figure 14.4.1. SCA Simplified Block Diagram

14.4.2.1 **CPU CCA's A1 and A2.** The SCA contains two CPU's and other data processing CCA's in a VME rack. The VME rack printed-wiring backplane contains 2 rows of board connectors: one for the 32-bit VME data bus, and one for interconnections and operating voltages. The two CPU CCA's are similar and provide redundancy. One CPU CCA serves as the primary processor while the second CPU CCA is in standby. Each CPU monitors the other processor. If the primary processor fails a self-test, it is automatically switched offline and the backup CPU assumes the role of primary.

Two pushbuttons (RESET and ABORT) are mounted on the front frame of the CPU CCA: these switches are not used in the field. ABORT halts program execution without resetting the CPU. In the event that ABORT is inadvertently pressed, press RESET to reset the CPU's and activate SYSRESET which resets all other VME boards. Resetting the CPU does not affect DRAM contents.

The following paragraphs describe the CPU functional block diagram (figure 14.4.2). Each CPU CCA contains:

- ! A 68010 series microprocessor running at 10 MHZ
- ! EPROM
- ! Dynamic random access memory (DRAM)
- ! Two RS-232 ports
- ! A 16-bit timer

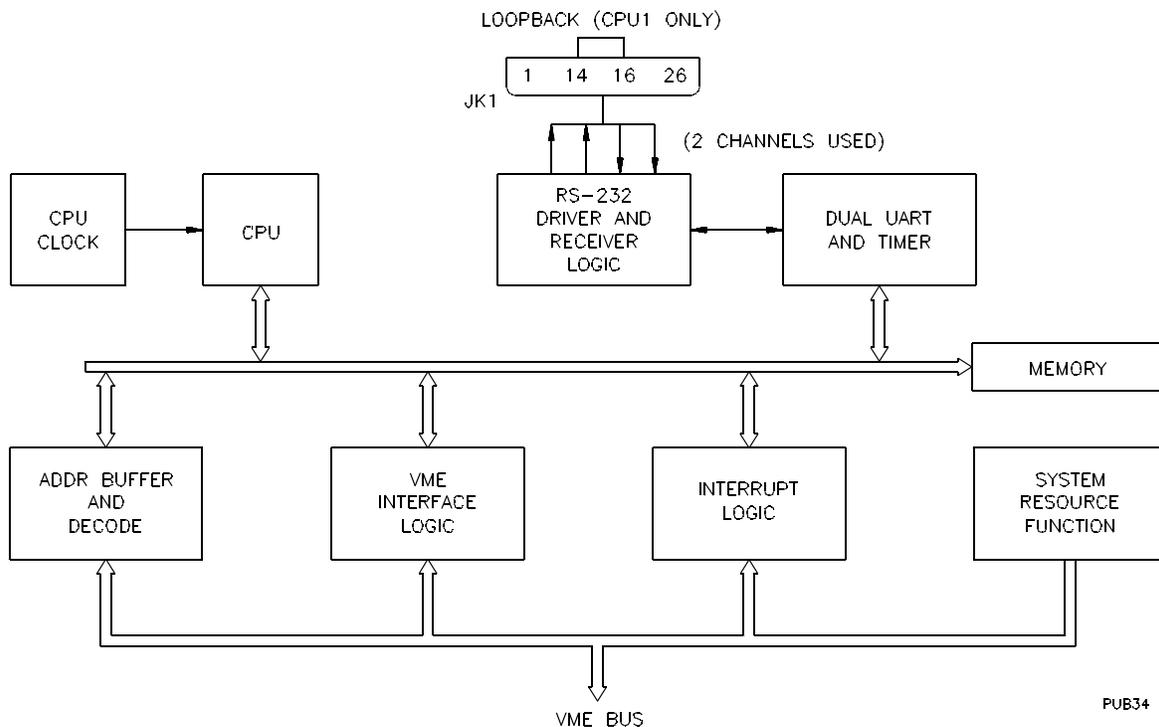


Figure 14.4.2. CPU, Simplified Block Diagram

During system operation one CPU CCA is the primary CPU that performs all processing and I/O functions while the other CPU functions in standby. Initially CPU #1 is the primary CPU.

The CPU CCA consists of nine functional areas: system resource function, two dual universal asynchronous receiver-transmitters (UART's), timer, RS-232 transmitter-receiver, CPU clock, microprocessor, interrupt

logic, VME interface logic, address buffer and decoder, and memory. The system resource function on the primary CPU provides system clock, system reset, bus arbitration, bus timer and functions as the VME bus controller. The corresponding system resource function on the secondary CPU is not used unless it becomes the online CPU.

The dual UART's and timer provides two RS-232 serial communication channels, a timer, and two I/O and control ports. The RS-232 driver and receiver logic interfaces UART channels A and B to external devices via connector J1 on the CPU by providing standard transmit and receive lines. (CPU's #1 and #2 each provide two additional UART channels that are not presently used.) CPU #1 is connected as the primary CPU with a loopback jumper installed between channel B transmit and receive lines (JK1 pins 14 and 16). When power is applied both CPU's issue a message from their respective UART channel B. CPU #1 immediately receives this message via the loopback jumper installed on the CCA front panel connector JK1. Both CPU's examine their receive lines and CPU #1 detects that it has received the loopback signal and assumes the role of the online CPU. Conversely, when CPU #2 detects that it has not received the loopback signal, it assumes the role of the standby CPU. The standby CPU continuously monitors CPU status by examining a location on the memory board where a tally count is stored. The online CPU updates this count on a periodic basis. Failure to update the count indicates a CPU failure which causes the standby CPU to become the primary CPU. The CPU operates from an internally generated 10 MHZ clock to execute ASOS operational firmware in the memory board EPROM's. Interrupt logic monitors the dedicated interrupt lines and informs the CPU when an interrupt line is active. The interrupts are prioritized and processed on a first-come, first-serve basis. VME interface logic provides standard address, data, and control signals for system bus communication.

The address buffer-decoder addresses all devices for microprocessor read/write operations. CPU onboard memory consists of 128K bytes of EPROM and 512K bytes of DRAM. Refresh circuitry for the DRAM is not disabled during a RESET; therefore, the CPU may be reset without affecting memory contents. The SCA continuous self-test (CST) checks CPU status once per minute; results are displayed on the CPU page of the OID. The CST checks the following areas of both CPU's:

- ! DRAM
- ! EPROM
- ! BUS ERRORS
- ! SERIAL PORTs #1 and #2 LOOPBACK
- ! SERIAL PORTs #1 and #2 XMIT ERRORS

For the online CPU, test pass/fail status is displayed for each functional areas. The backup CPU test status is displayed for the overall board. The technician can manually run the CPU test from the CPU page at any time. A "T" status is displayed for each test category until the test is rerun during the next CST cycle. After each cycle, test status is updated and displayed, and the fail count (if applicable) is incremented.

The DRAM test is based on an alternating pattern of addressing memory locations. Data output to the DRAM are read back and evaluated, and the test status is then displayed. The EPROM test is based on a checksum. The checksum is compared to the last byte in the EPROM, the result is evaluated, and test status is displayed. The BUS ERRORS test is based on a memory write to a specific address; contents of the addressed memory location are evaluated, and test status is displayed. SERIAL PORT #1 and #2 LOOPBACK tests ensure that the CPU can communicate with its internal UART. The CPU reads the UART interrupt vector register and checks for bus errors.

Test status is displayed as "P" (pass) if no bus errors occur. For SERIAL PORTs #1 and #2 XMIT ERRORS test, the CPU reads the contents of the status register for the corresponding port. This register contains information on transmission errors detected by the UART during RS-232 communications. Specifically, the CPU checks the status register for parity errors, framing errors, and overrun errors that might have occurred.

If such errors occur for three consecutive CST cycles, an "F" (fail) is displayed for test status; otherwise, test status is "P" (pass).

14.4.2.2 **Memory Board A3.** As shown on the memory board block diagram (figure 14.4.3), the VME-110 memory board contains three memory banks. Each bank is independently configured via jumpers to specify VME address/memory chip size, device speed, device pinout, and backup power. The following paragraphs provide a detailed block diagram description of the memory board. (Digitized voice input is stored in Voice Audio Board A21.) The memory board includes nine functional areas: banks 1, 2, and 3 memory devices; VME/bank address decode and control; battery backup; data buffer; bus cycle control; address buffer and decode logic; and system real-time clock. The first bank contains up to 4 megabytes of EPROM which stores the operational software program run by the CPU.

Bank 1 also stores data collection package (DCP) software load that is transferred to the DCP in the event that a DCP loses its program load and requires initialization. Banks 2 and 3 contain up to 2 megabytes of static random access memory (SRAM). SRAM provides storage for ASOS weather archives. Address and control signals used to address memory locations are generated by the VME/bank address decode and control. The memory boards are configured with a battery backup to provide an alternate power source in the event of a power loss.

The data buffer, bus cycle control, and address buffer and decoder provide standard address, data, and control signals for system bus communication. The real-time clock maintains clock calendar timing, which is accessed by the CPU upon initialization. When initialized, the CPU maintains a real-time clock via software.

The SCA CST checks status of the memory board once per minute. CST results are displayed on the memory page of the operator interface device (OID). CST performs an EPROM test and an SRAM test. The technician can manually run the memory test from the memory page at any time. "T" status is displayed for each test category until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The EPROM test is based on a checksum, which is compared to the last byte in the EPROM. The result is evaluated and the test status is displayed. The SRAM test ensures that the CPU can read data from the SRAM on the memory board without encountering bus errors.

14.4.2.3 **Serial I/O (SIO) Boards A5 through A11.** Seven serial I/O (SIO) boards communicate with other equipment. SIO #1, A5, communicates in RS-422 format, while the remaining six boards all use the RS-232 format. The SIO boards communicate with the CPU on a character-by-character basis. The CPU must process interrupts on each and every transmitted and received character. The detailed block diagram of the SIO board (figure 14.4.4) is described in the following paragraphs.

The SIO board consists of six functional areas: two serial communication controllers (SCC's), interrupt logic, data buffer, bus cycle control, and address buffer and decode logic. The SCC's provide a variety of communication modes. Upon power up, the CPU initializes the SCC's to the proper communication modes.

Interrupts are generated via the interrupt logic. An interrupt could signify that a received character is available, that the transmit buffer is empty, or that an external status change has occurred.

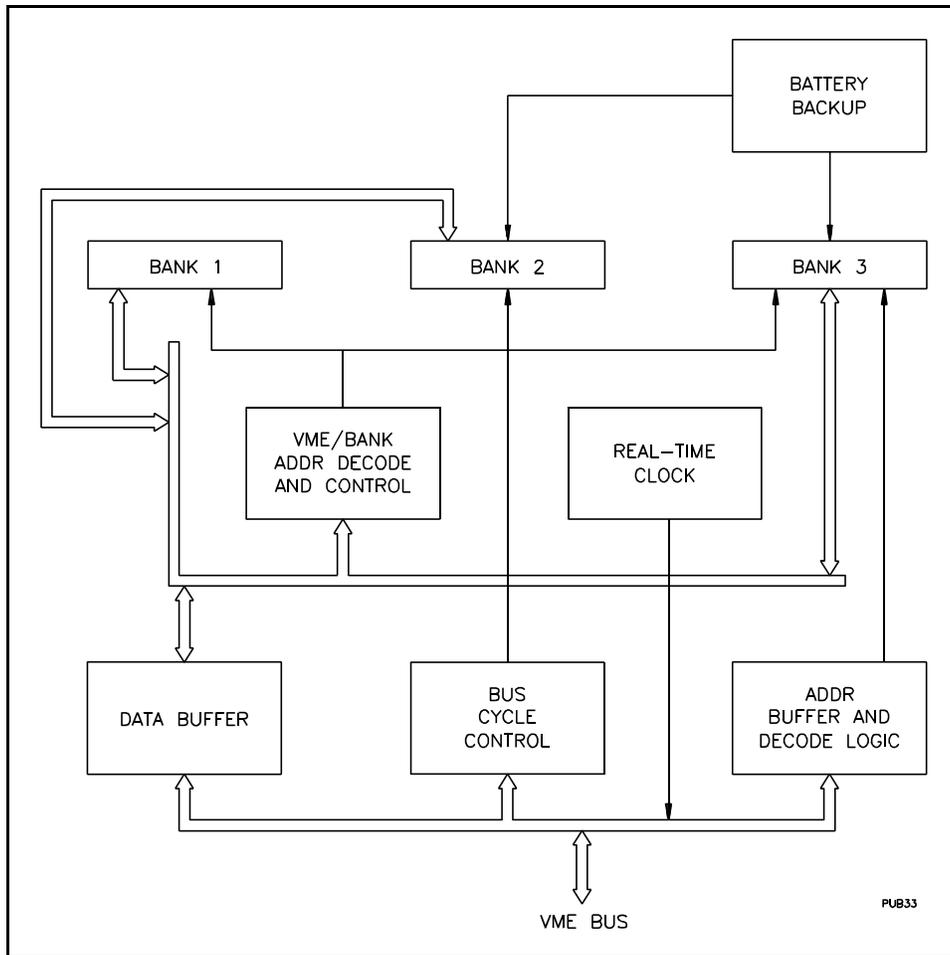


Figure 14.4.3. Memory Board, Functional Block Diagram

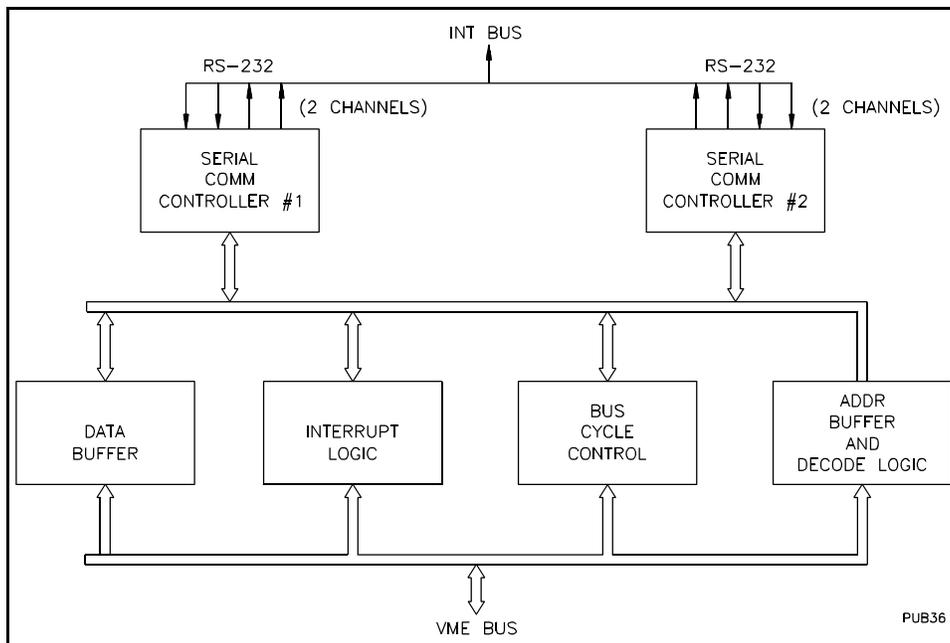


Figure 14.4.4. SIO Board, Functional Block Diagram

The data buffer, bus cycle control, and address buffer and decoder logic provide standard address, data, and control signals for system bus communication.

The four ports of SIO boards 1 through 3 are factory assigned to specific devices. Their ports are dedicated to these devices via corresponding connectors on the SCA main wiring harness. Although these ports can be reassigned via the SCA serial communications page of the OID, the technician should not reassign them; assigning these ports to other field replaceable units (FRU's) would invalidate their corresponding harness markers. Table 14.4.1 identifies each port of the SIO boards and lists the corresponding harness connector and device to which it is connected.

Unlike SIO boards 1 through 3, SIO boards 4 through 8 are installed only as required depending upon sensor complement. Most systems will not have all 8 SIO boards installed. The ports of SIO boards 4 through 8 are not factory assigned to specific devices. Rather, these ports are assigned to various devices during the initial configuration of the system. This assignment is made via the SCA serial communications page of the OID.

Table 14.4.1 identifies the ports of SIO boards 4 through 8 and identifies the W106 connector that corresponds to each. The devices attached to the connectors correspond to the device assigned to that port by the SCA serial communications page. Figure 14.4.5 identifies pin-to-pin wiring with signal function between each of the SIO boards and their respective connectors. §

Table 14.4.1. SIO Port Assignments

SIO	Data Format	Ref Des	Interface	Function
1-1	RS-422	7A1A1A2A5	P59	FAA
1-2	RS-422	7A1A1A2A5	P60	FAA
1-3	RS-422	7A1A1A2A5	P61	FAA
1-4	RS-422	7A1A1A2A5	P62	FAA
2-1	RS-232	7A1A1A2A6	P13	RF Modem #1
2-2	RS-232	7A1A1A2A6	P14	Pressure #1
2-3	RS-232	7A1A1A2A6	P15	User #1 (A1A9)
2-4	RS-232	7A1A1A2A6		Voice
3-1	RS-232	7A1A1A2A7	P16	RF Modem #2
3-2	RS-232	7A1A1A2A7	P17	Pressure #2
3-3	RS-232	7A1A1A2A7	P18	User #2 (A1A10)
3-4	RS-232	7A1A1A2A7	A1A3J1	Primary OID
4-1	RS-232	7A1A1A2A8	P20	(UPS)
4-2	RS-232	7A1A1A2A8	P21	Pressure #3
4-3	RS-232	7A1A1A2A8	P22	*
4-4	RS-232	7A1A1A2A8	P23	*
5-1	(IAW sensor)		P1M/W A3A1J1	Sensor #1
5-2	(IAW sensor)		P2 M/WA3A2J1	Sensor #2
5-3	(IAW sensor)		P3 M/WA3J1	Sensor #3
5-4	(IAW sensor)		P4 M/W A4J1	Sensor #4
6-1	(IAW sensor)		P5 M/W A5J1	Sensor #5
6-2	(IAW sensor)		P6 M/W A6J1	Sensor #6
6-3	(IAW sensor)		P7 M/W A7J1	Sensor #7
6-4	(Not used)		P8 M/W A3A8J1	*Sensor #8

Table 14.4.1. SIO Port Assignments -CONT

SIO	Data Format	Ref Des	Interface	Function
7-1	RS-232		P24	
7-2	RS-232		P25	
7-3	RS-232		P26	
7-4	RS-232		P27	

* Customer Option

The SCA CST checks the status of the SIO boards once per minute. CST results are displayed on the SCA SIO display pages of the OID (one page for each SIO board). The CST performs the LOOPBACK test and XMIT ERRORS test on each of the four ports of an SIO board. The technician can manually run the SIO test from an SIO page at any time. "T" status is displayed for both test categories until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

For the LOOPBACK test, the CPU reads an interrupt vector register on the SIO board to ensure that it can communicate with the SIO port. For the XMIT ERRORS test, the CPU reads the contents of the SCC status register for the corresponding port. This register contains information on transmission errors detected by the SCC during RS-232 communications. Specifically, the CPU checks the status register for parity errors, framing errors, and overrun errors that may have occurred. For both LOOPBACK and XMIT ERRORS tests, CST status is displayed as either P (pass), F (fail), or D (degraded). A status of D is displayed if five or more errors have been detected and the port is currently passing the test. At 0600 LST each day, the number of accumulated failures is summarized in the system (maintenance) log.

14.4.2.4 **A/D Board A13.** The A/D board, shown functionally on figure 14.4.5, monitors power supply outputs and quantifies them to provide digital measurements for data processing. From voltage divider networks on the VME resistor board, the A/D board receives dc voltage samples and converts them to digital values to be read by the CPU via the VME bus.

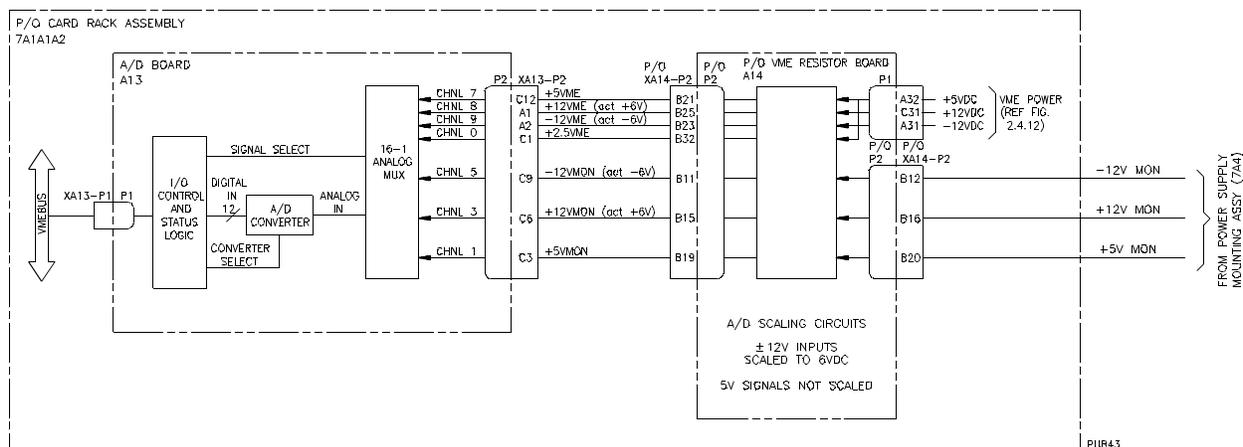


Figure 14.4.5. A/D Board, Functional Block Diagram

14.4.2.5 **VME Resistor Board A14.** The VME resistor board mounts discrete resistors used by the other VME CCA's for pull-ups, loads, and voltage dividers and a precision voltage source for the A/D board. §

14.4.2.6 **DIO Board A15.** The digital I/O (DIO) board, shown functionally on figure 14.4.6, provides address buffer and control, data buffer, timing and interrupt control, two dual I/O data port integrated circuits (IC's) (#1 and #2), and four data transceiver IC's. The DIO board has an input bit that selects SCA mode of operation (APCSEL). §

The DIO board communicates with the CPU via the address buffer and decoder, data buffer, and timing and interrupt control logic. Two dual I/O port IC's provide a total of four ports (designated A1, B1, A2, and B2), each of which communicates with external devices via a dedicated data transceiver IC. Configured as an input-only port, A1 is used by the CPU to input a watchdog timer signal from the Voice Processor Board A20, status bits for the dc power supplies (via the VME Resistor Board A14), and the UPS bypass circuit. Port B1 is configured as an output-only port. This port is used by the CPU to output control signals to the voice recorder/playback board, the rf modem switch (or line driver relay), and the UPS bypass circuit. (Two additional ports on the DIO board, A2 and B2, are not used in the SCA.) Notice that the SCA CST does not check status of the DIO board. §

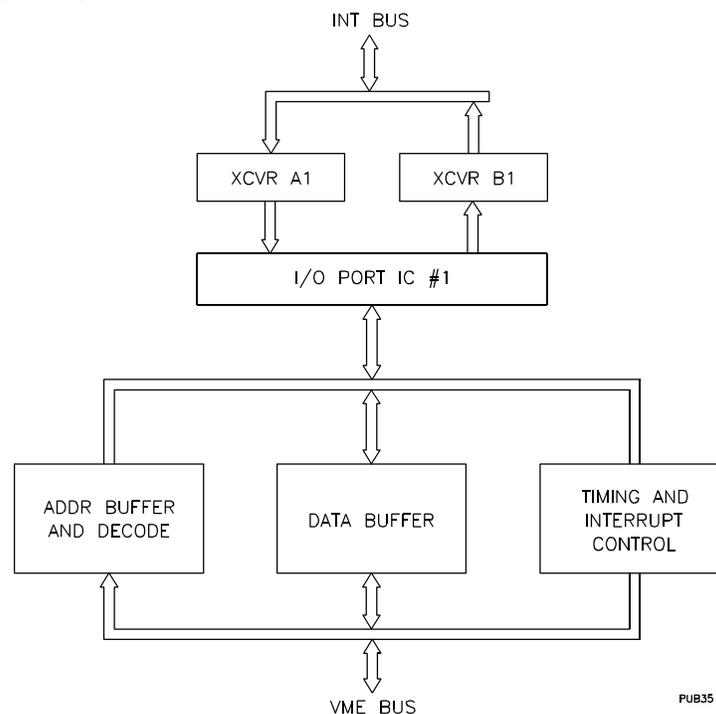


Figure 14.4.6. DIO Board, Function Block Diagram

14.4.2.7 **Digitized Voice Processor System.** As shown in figure 14.4.7, the digitized voice processor subsystem includes Voice Processor Board A20 and Voice Audio Board A21. These two boards operate together as a system and are tested together. Both boards are connected to the VME bus for power and system reset purposes, but they do not communicate with the CPU via the VME bus. The CPU/voice system communication is accomplished via the RS-232 link between SIO board #2 and the voice processor board. Digital voice processing consists of three operations:

- ! Recording an operator-generated addendum up to 90-seconds long
- ! Using a stored vocabulary of voiced words to assemble a verbal report in accordance with current ASOS data
- ! Producing an output message consisting of the verbal report plus the addendum.

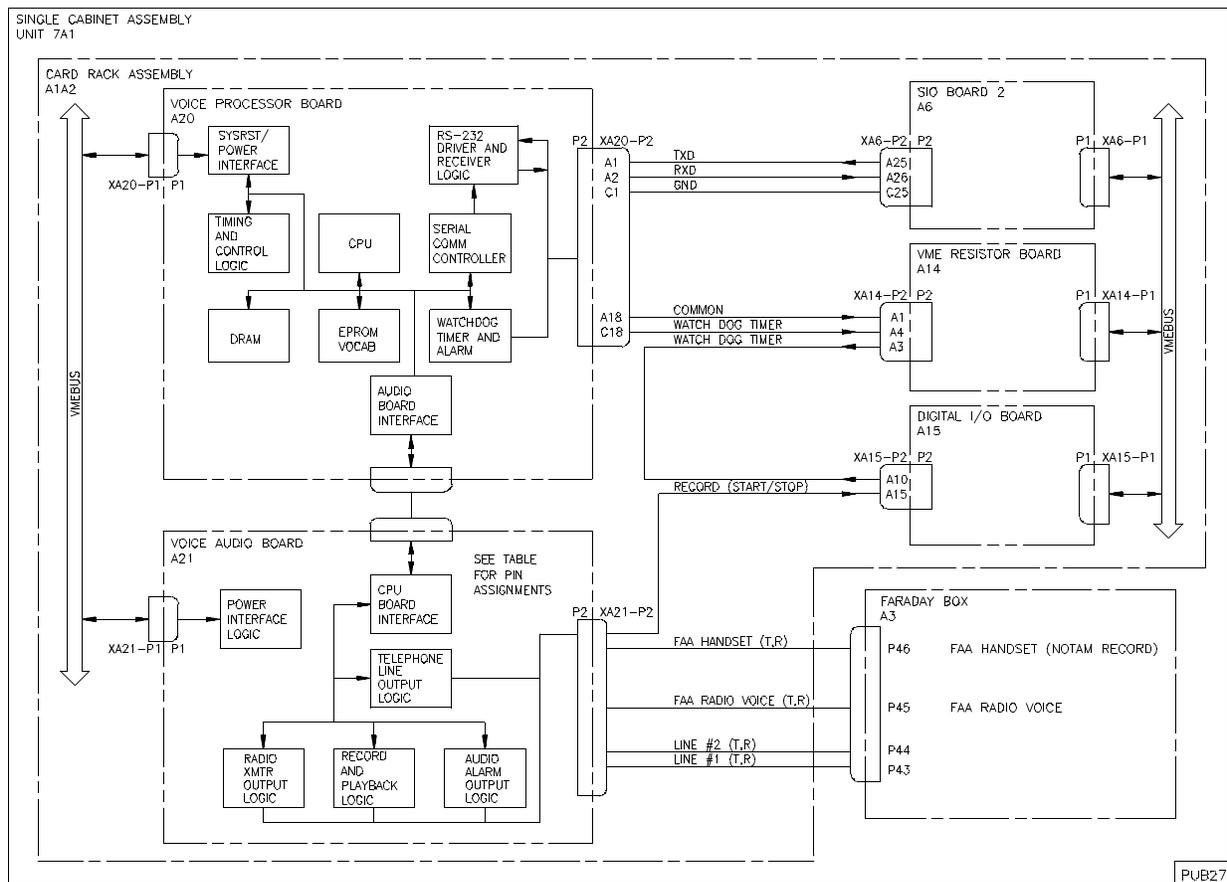


Figure 14.4.7. Digitized Voice Processor, Functional Block Diagram

14.4.2.7.1 Voice Processor Board A20. The voice processor board contains a Z80XXX series (Z80 thousand series) microprocessor and the necessary DRAM to execute the firmware stored in onboard erasable programmable read only memory (EPROM). These instructions reconstruct digitized human voice, create voice reports, and receive operator-generated digitized audio from the voice audio board. The voice processor board communicates with the VME bus directly for power and system reset but indirectly via SIO board #2 for system communication. The following paragraphs provide a detailed block diagram description of the voice processor board. The voice processor board consists of nine functional areas: system reset/power interface, DRAM, EPROM vocabulary, CPU, audio board interface, timing and control logic, serial communications controller, RS-232 driver and receiver logic, and watchdog timer and alarm. Upon receipt of a system reset signal from the VME bus, when the RESET pushbutton (on the front of the CCA) is pressed, or when power is applied, the system reset/power interface logic generates an internal reset. This internal reset disables message broadcast until a play message string is received from the CPU via SIO board 2. The VME bus interface for power and ground requirements is also provided by the system reset/power interface. DRAM provides 1 megabyte of memory for message/file storage: this is the memory area where digitized voice messages from the FAA handset are stored. These messages are appended to the automatically generated observation messages. The EPROM vocabulary consists of 512 kilobytes of EPROM for voice files.

Voice Processor Board A20 executes the operational software to execute new message strings and to monitor the eight telephone lines. Interface between Voice Processor Board A20 and Voice Audio Board A21 is provided by 50-pin connectors on the front of the boards and a ribbon cable. Timing and interface signals required by the CPU and peripherals are provided by the timing and control logic section of Voice Processor Board A20. The serial communications controller provides the RS-232 serial communication channel, while the RS-232 driver and receiver logic section provides the standard RS-232 receive and transmit lines. The watchdog timer and alarm provides an alarm signal to the primary CPU (via Digital I/O Board A15) whenever a CPU software or hardware failure occurs.

14.4.2.7.2 Voice Audio Board A21. Voice Audio Board A21 receives digitized voice from Voice Processor Board A20 and converts it into audio. Audio is output as a weather data message for dial-in weather requests and is broadcast by a ground-to-air (GTA) radio transmitter for aviation use. In addition, the voice audio board receives voice audio from the FAA handset, quantifies it, and transmits digitized audio to Voice Processor Board A20 for message processing. The following paragraphs provide a detailed block diagram description of Voice Audio Board A21 which consists of six functional areas: CPU board interface, power interface logic, radio transmitter output logic, record and playback logic, telephone line output logic, and audio alarm output logic.

Pinouts for the output of the voice audio board (XA21-P2) are provided in table 14.4.2. The signal mnemonics and pins associated with row A and row C of XA21-P2 are listed with the associated plug connector. For example, the RING signal of the FAA handset line can be monitored at pin 20 of XA21-P2 or pin 2 of plug 46 (P46). The CPU board interface provides the communication path to the voice processor board via the 50-pin connector on the front of the board. The VME bus interface for power and ground requirements is provided by the power interface logic. Radio transmitter output logic and record and playback logic digitize audio input and synthesize digitized voice words to form audio clauses or sentences. Interface circuits to the telephone outputs and line output peripherals are provided by the telephone line output logic section. The audio alarm output logic section drives an audio ALARM indicator. One of the audio line outputs is continually monitored by the alarm circuit. A loss of audio for a predetermined period causes the indicator on Voice Audio Board A21 to illuminate. Chapter 12 provides information on GTA radio pin-to-pin connections.

Table 14.4.2. Digitized Audio Connections

Function	I/O Conn	VME Rack 7A1A1A2-	Signal Mnemonic
Call-in Line #1, ring	P43-2	XA21P2-A32	L1-RING
Call-in Line #1, tip	P43-3	XA21P2-C32	L1-TIP
Call-in Line #2, ring	P44-2	XA21P2-A31	L2-RING
Call-in Line #2, tip	P44-3	XA21P2-C31	L2-TIP
FAA Radio, ring	P45-2	XA21P2-A24	FAA RADIO RING
FAA Radio, tip	P45-3	XA21P2-C24	FAA RADIO TIP
NOTAM Record, ring	P46-2	XA21P2-A20	NOTAM RECORD RING
NOTAM Record, tip	P46-3	XA21P2-C20	NOTAM RECORD TIP

14.4.2.7.3 Digital Voice Processing System Self-Tests. The SCA CST checks the status of the digital voice processing system once per minute. CST results are displayed on the voice page of the OID. The CST performs four tests on the voice processing system: CPU, AUDIO OUTPUT, AUDIO STATUS, and TIMEOUT. At any time, the technician can manually run the voice processing test from the VOICE page. A "T" status is displayed for the four test categories until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented. The CPU test checks operational status of the voice processor board. The TIMEOUT test checks operational status of

the watchdog timer. The AUDIO OUTPUT and AUDIO STATUS tests check operation of the voice audio board and indirectly test the voice processor board. The AUDIO OUTPUT test is based on an internal audio test that checks audio circuitry. The AUDIO STATUS test is based upon a monitored audio line. The status of each of these tests is evaluated and test status is displayed.

14.4.2.8 **Pressure Sensor Shelf 7A1A1A7.** Pressure sensor shelf 7A1A1A7 mounts either two or three identical atmospheric pressure sensors. Cable W106 provides the electrical connections to the sensors as shown on figure 14.4.8. Plastic vent tubes from each sensor are joined under the pressure shelf to a tube cross and then routed to the pressure port at the top of the cabinet. Because the SCA is installed outdoors, a temperature sensor board (7A1A1A7A4) is mounted on the front of the pressure sensor shelf to monitor internal cabinet temperature. The board sends an analog temperature signal to the processor via A/D Board A2A13 to be used in the pressure algorithms.

14.4.3 AC POWER DISTRIBUTION

AC power service entrance into the SCA is through a stuffing tube in the bottom of Faraday Box A3; termination is to terminal blocks A3A17 and A3A18, which are mounted on the back side of the hinged front cover. AC power is routed to Power Reset Assembly A1A13 (figure 14.4.8A) which delays power application for three seconds before distributing the power to SCA assemblies (Class I systems) or the UPS bypass circuit (Class II systems). The Class II SCA UPS bypass circuit consists of a power relay (which routes site power or UPS output to SCA assemblies) and a digital I/O module (which provides ASOS operational software with UPS bypass monitoring and control).

As shown on figure 14.4.9, Faraday box connectors J1, J2, and J3 apply power to the main SCA cable harness W106. J1 supplies power through main circuit breaker A1A3CB1 (via the UPS bypass circuit in Class II systems). Connector A3J3 provides heater power for primary sensors (sensors 1-4). Connector A3J9 provides cabinet heater power. Connector A3J10 provides heater power for the aux box. AC power for aux box components is provided through short conduits from Faraday Box 7A1A3. The aux box is installed with most Class II single-cabinet systems, but is an available option on Class I and reduced capability systems. A secondary UPS, 7A2A1A6, is an option for installation in the aux box.

14.4.3.1 **Power Reset Assembly A1A13.** Power from the power distribution assembly is routed to Power Reset Assembly A1A13 Time Delay Relay K1 (figure 14.4.9 sheet 4) which provides a three second delay before distributing the power to the SCA assemblies (Class I systems) or UPS bypass circuit (Class II systems). The three second delay enables the pressure sensors and rf modems to reset after power is interrupted. In Class II systems, the UPS bypass circuit consists of Digital I/O Module K2 and Power Relay K3. Power from Time Delay Relay K1 is applied to Power Relay K3 normal closed contacts and to UPS A1A6. Power to Power Relay K3 normally closed contacts is routed to the AC Power Distribution Assembly where it is distributed to the SCA assemblies. UPS output power is routed to Power Relay K3 normally open contacts.

After power is applied to the SCA assemblies, ASOS operational software monitors the bypass status of Power Relay K3 via Digital I/O Module K2 and Digital I/O Board A1A2XA15. When UPS A1A6 status is good, Power Relay 7A1A1A13K3 is energized (via Digital I/O Board A1A2XA15 and Digital I/O Module A1A13K2) which enables UPS output power to be distributed to the SCA assemblies. During turn on and when the UPS status is bad, the power relay is deenergized allowing site power to be applied directly to the SCA assemblies.

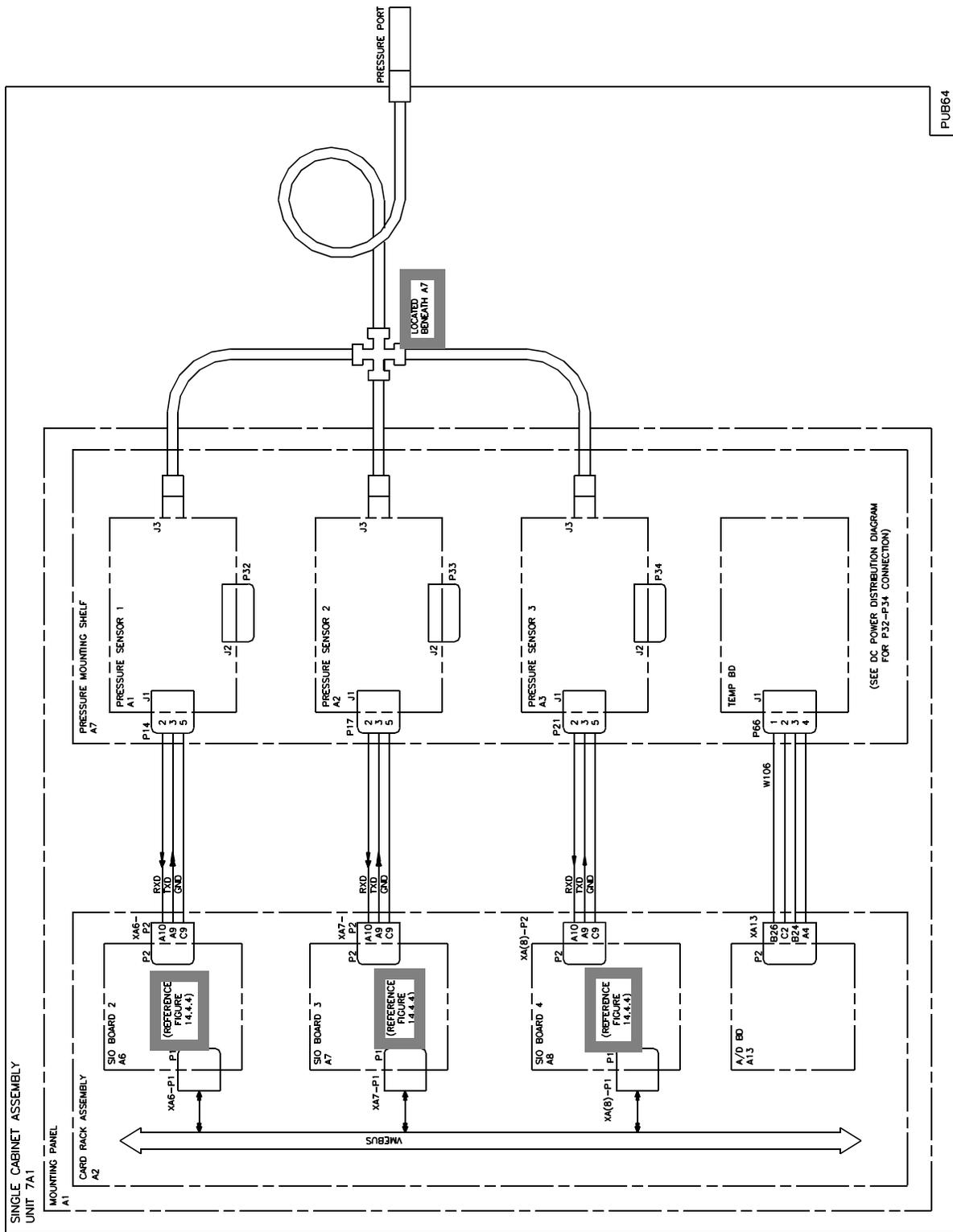
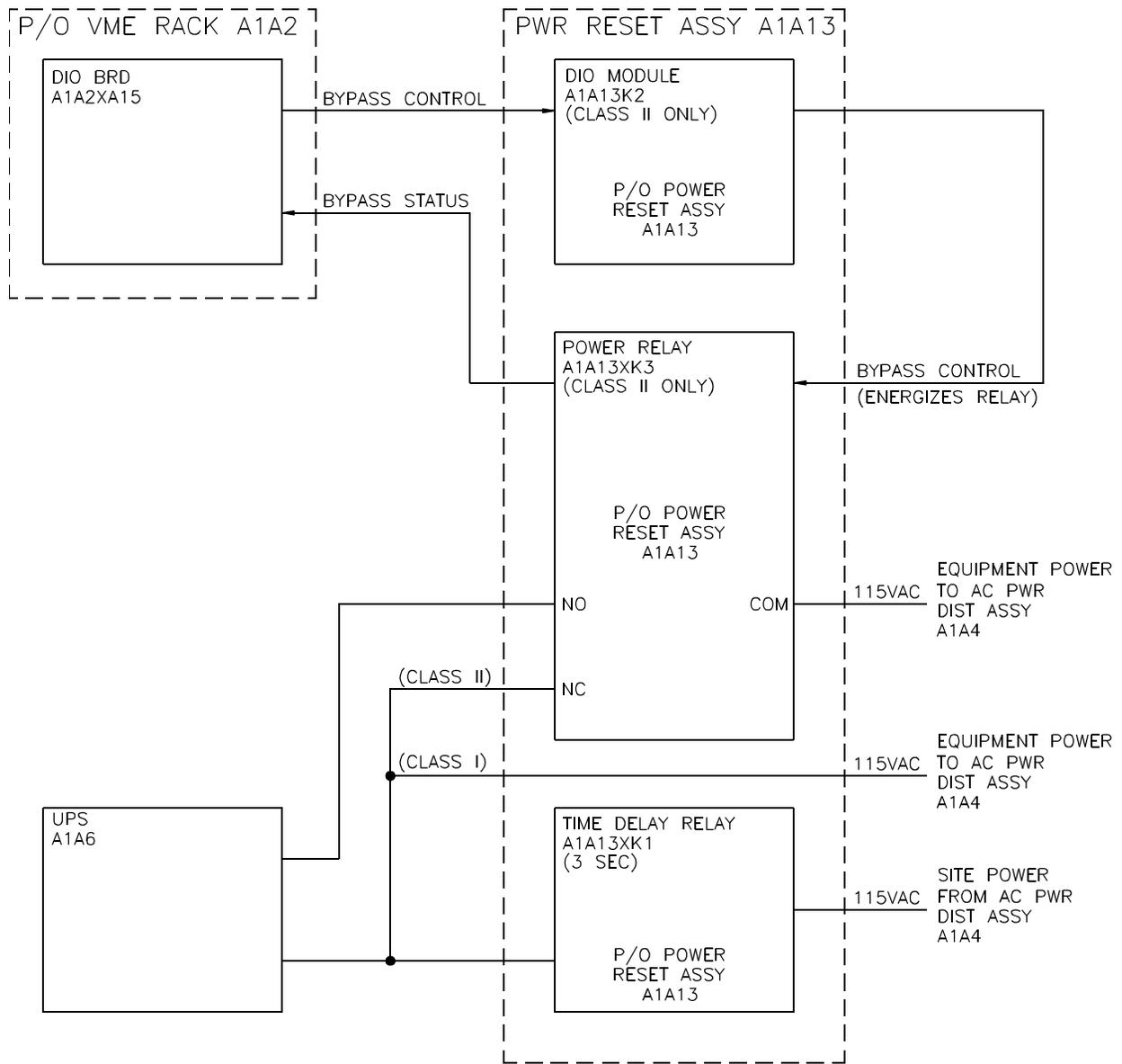


Figure 14.4.8. Pressure Sensor Shelf, Functional Diagram



PUB71

Figure 14.4.8A. SCA Power Reset Assembly

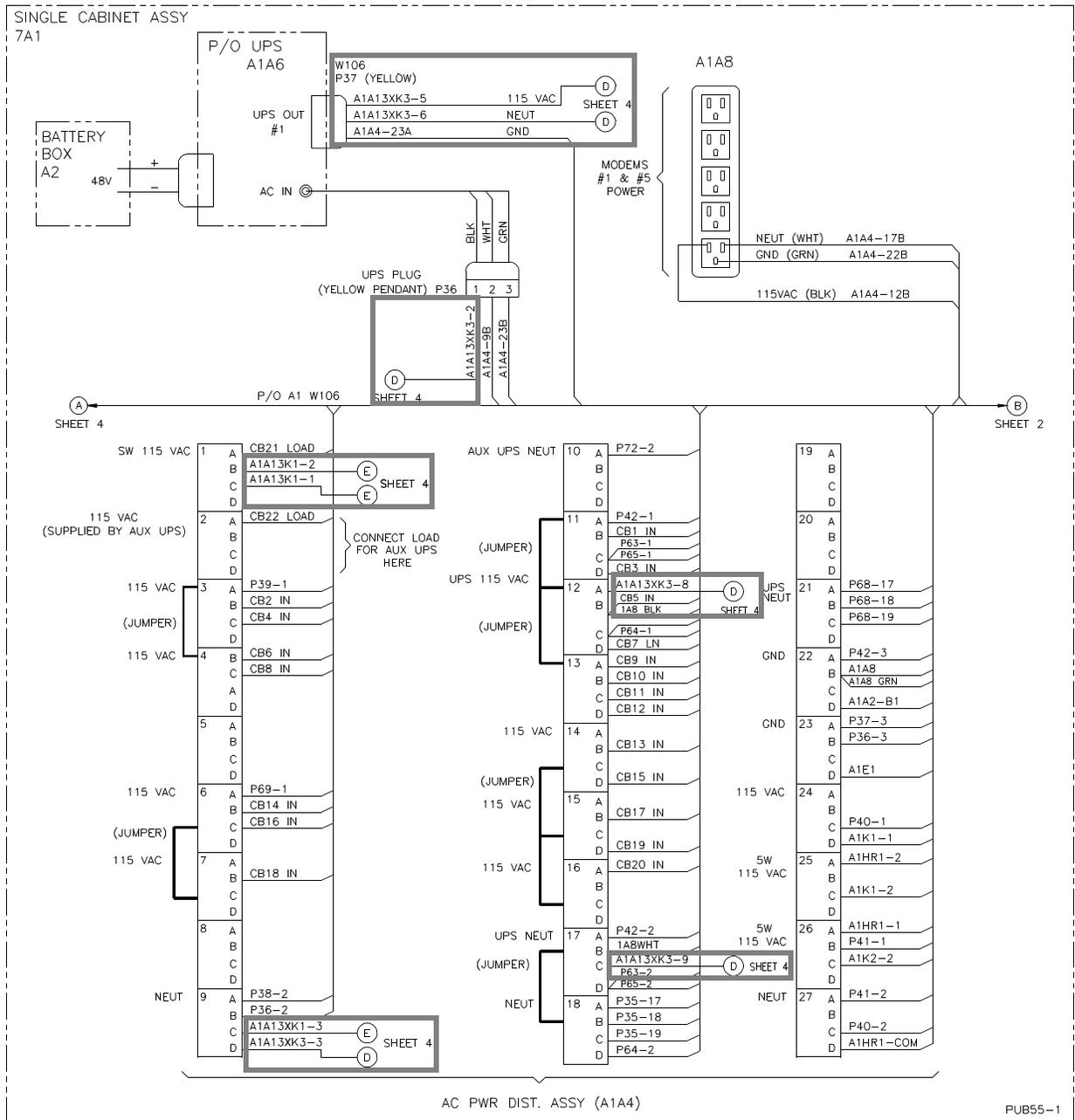


Figure 14.4.9. AC Power Distribution Diagram (Sheet 1 of 4)

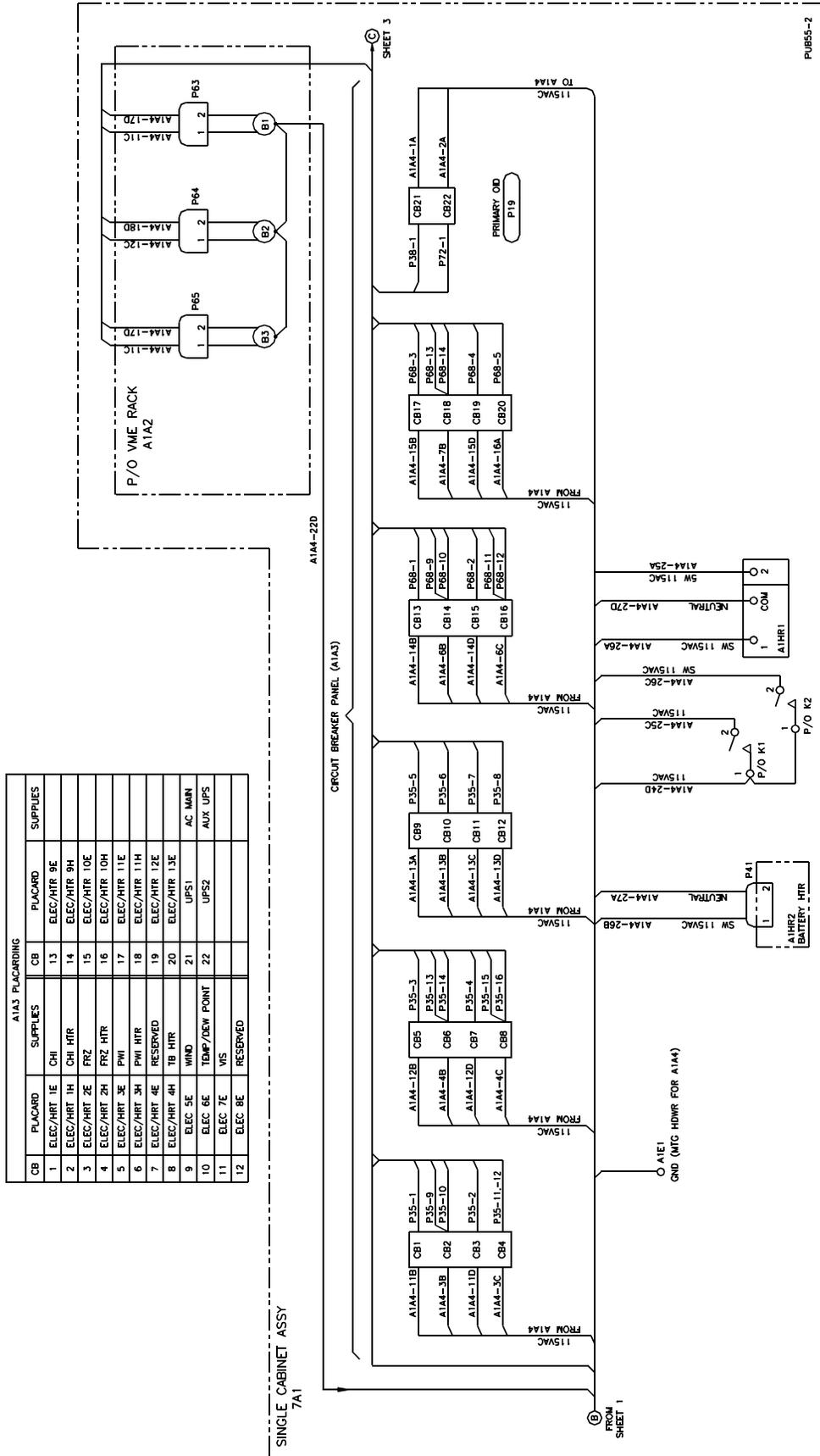


Figure 14.4.9. AC Power Distribution Diagram (Sheet 2)

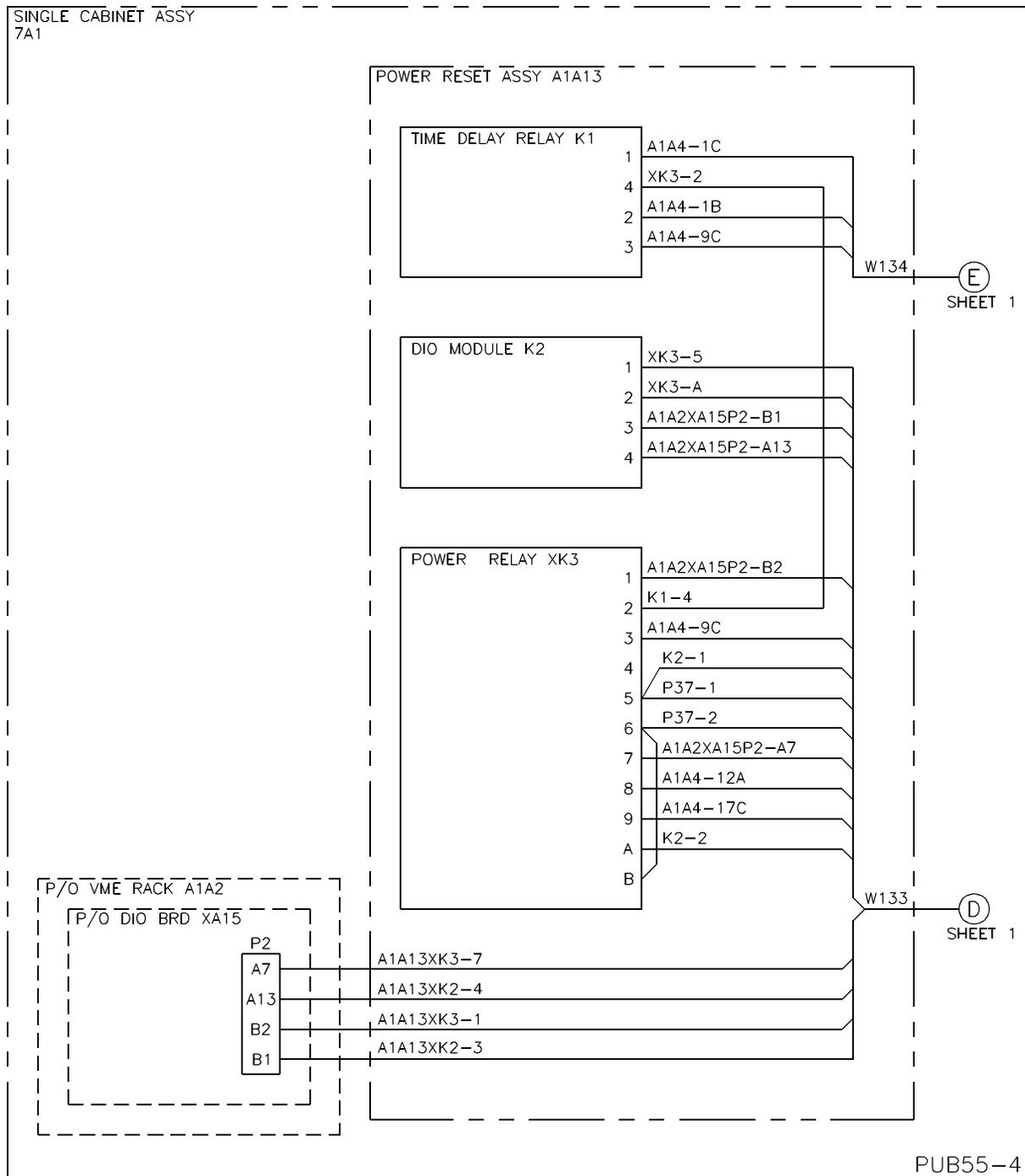


Figure 14.4.9. AC Power Distribution Diagram (Sheet 4)

14.4.4 SCA CABINET HEATERS

Because the SCA must operate out-of-doors in all climatic conditions, electrical heaters are included to ensure accurate, reliable operation in cold weather. As shown on figure 14.4.10, separate heaters are mounted on the 7A1A1 mounting assembly, with cabinet heater 7A1A1HR1 behind Circuit Breaker Panel 7A1A1A3, and battery heater 7A1A1HR2 at bottom left of Mounting Panel 7A1A1. These heaters operate from 115 vac which is applied through solid-state relays 7A1A1K1 and 7A1A1K2. The relays are controlled by three thermostatic switches, which also are mounted on 7A1A1 behind the circuit breaker extrusion. Cabinet heater 7A1A1HR1 includes two 325-Watt heating elements (metal strips), while 7A1A1HR2 is a 350-Watt silicon strip. When ambient temperature in the cabinet falls to 60°F, thermostatic switch 7A1A1S1 closes to apply +5V to 7A1A1S2 and 7A1A1S3. If the temperature falls to 50°F, S3 closes to energize relay 7A1A1K2 and 7A1A1S2 closes to energize relay 7A1A1K1. Relay 7A1A1K2 contacts then applies 115 vac power to heater 7A1A1HR2 and one element of cabinet heater 7A1A1HR1. Relay 7A1A1K2 contacts apply 115 vac to the other half of cabinet heater 7A1A1HR1. At 70°F S2 and S3 open to deenergize relays K1 and K2. At 80°F, S1 opens to ensure removal of all heating power.

§
§
§
§
§

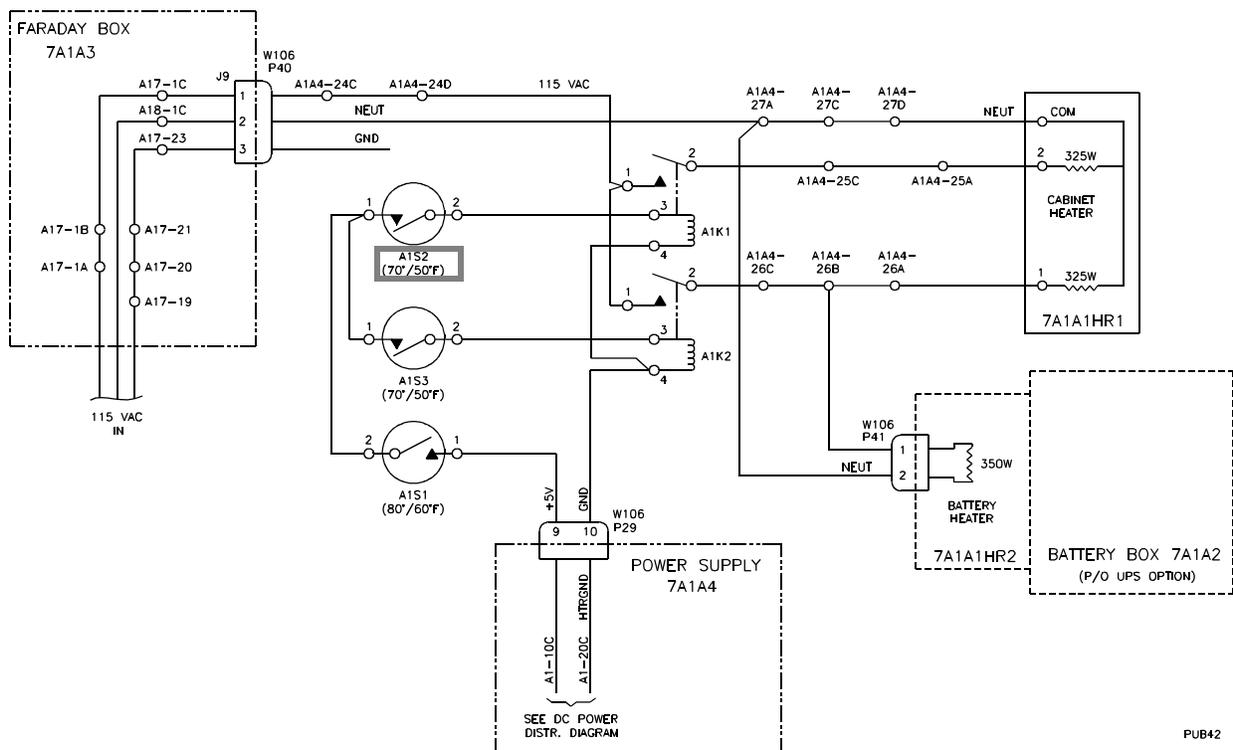
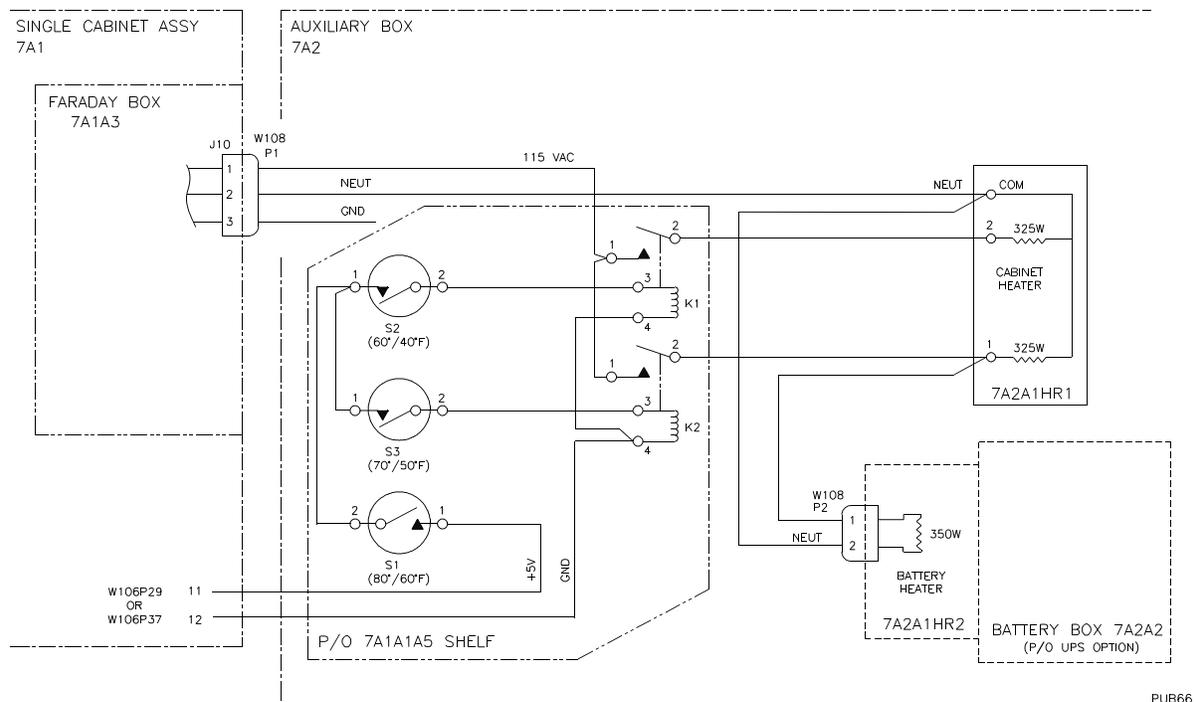


Figure 14.4.10. SCA Cabinet, Heater Control Circuit

14.4.5 AUXILIARY BOX CABINET HEATERS

The Aux box cabinet heater control circuit is shown in figure 4.4.11, and is similar to that in the SCA.



PUB66

Figure 14.4.11. Auxiliary Box, Heater Control Circuit

14.4.6 DC POWER DISTRIBUTION AND MONITORING

Figure 14.4.12 illustrates dc power distribution within the SCA. DC power for the SCA is provided by paired power supplies located in DC Power Supply Plate Assembly A4. These power supplies receive ac input power from UPS output (or bypass circuit) to provide +5 vdc, +12 vdc, and -12 vdc. Paired outputs are OR'ed together by diodes to ensure that one supply continues to provide power if the other fails and that the failed supply is isolated from the output line. AC input power to each of the four supplies is separately fused on DC Distribution Assembly A4A1, with 3.15A fuses F1 and F2 protecting PS1 and PS2, respectively, while 2.5A fuses F3 and F4 protect PS3 and PS4, respectively. The wiring harness for Power Supply Mounting Assembly A4 is designated W024.

Power supply output voltages are distributed from Power Distribution Assembly 7A1A1A4, shown on figure 14.4.13. There they are distributed by cable harness W024 (part of Power Supply Mounting Assembly A4) and wire harness W106, which interconnects the assemblies on Mounting Panel 7A1A1. To accommodate monitoring by system software, power supply outputs are connected to VME Resistor Board 7A1A1A2A14, which applies voltage samples to the A/D board for access. DC power applied to the rf modems is monitored in the same manner.

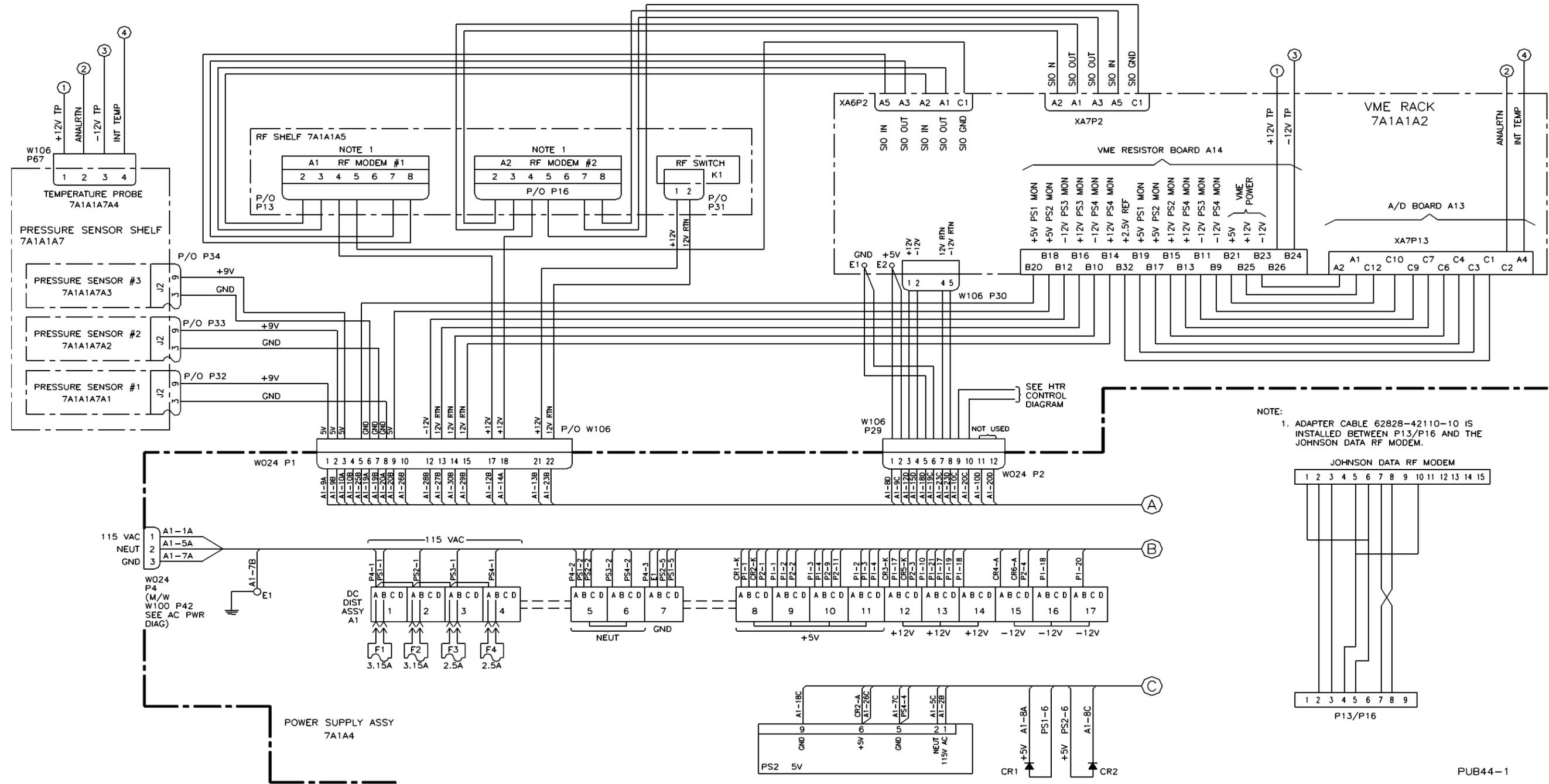
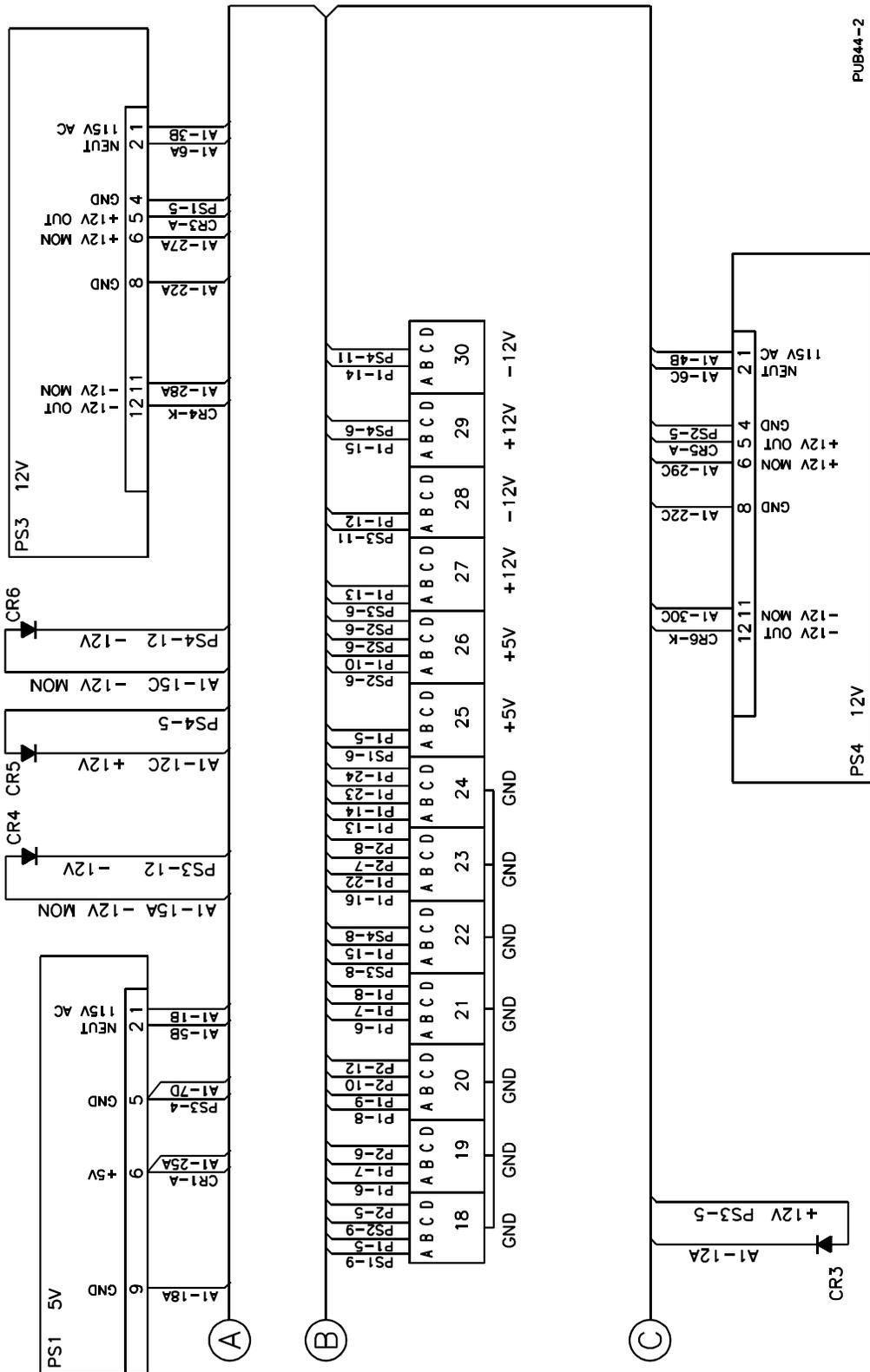
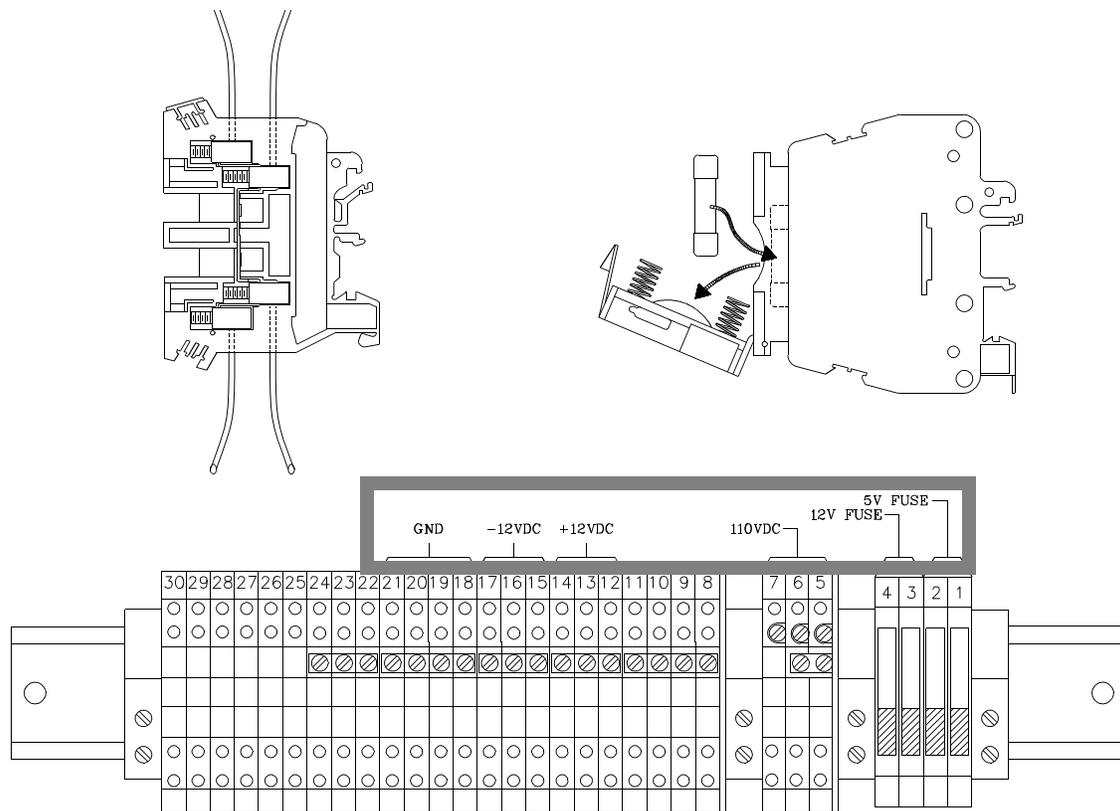


Figure 14.4.12. DC Power Distribution Diagram (Sheet 1 of 2)



PUB44-2

Figure 14.4.12. DC Power Distribution Diagram (Sheet 2)



PUB20

Figure 14.4.13. DC Power Distribution Assembly

14.4.7 SENSORS

- § The complement of sensors includes the pressure sensors that are mounted in the SCA and up to 13 additional sensors. Sensors are customer-selected to accommodate site requirements. Fiberoptic Transducer
- § Modules 7A1A3A1 through 7A1A3A13, located in the Faraday box, interconnect up to 13 sensors. These transducers are paired with identical transducers in the respective sensor cabinets. Each pair communicates in RS-232 format via fiberoptic cables. The SCA fiberoptic transducer modules connect through SIO Boards #5, #6, and #8 (A9, A10, and A12), each interfacing up to four modems.

The sensor complement installed at any particular site reflect requirements of that site as determined by the customer. Some sites may be provided with more than one type of sensor. Cloud height and visibility sensors are often duplicated at a site, with a maximum of three each possible. Usually, each touchdown zone is provided with cloud height and visibility sensors to ensure that current ceiling and visibility conditions at that specific runway are reported accurately.

14.4.8 PERIPHERALS

Peripheral devices are not supplied as standard equipment with the SCA. Any laptop PC can be connected to serve as an OID for maintenance purposes. The maintenance technician uses a laptop PC to check ASOS system status, to reconfigure the system, and to run on-demand diagnostic tests on specific elements of the system. Optionally, an OID and/or a video display unit (VDU) could be installed in an adjacent building, provided that it is within 200 feet of the SCA. All other outputs from ASOS are via direct connection (hardwire) or telephone modems. A modem also interfaces with the NWS Automation of Field Operations & Services (AFOS) system.

A digitized voice output is routed via phone modems to dial-in users (or via the GTA radio) to provide local weather and pressure data to pilots at or near the airport. The GTA radio continuously transmits current local meteorological observations on assigned VHF comm frequencies to pilots.

The FAA handset enables air traffic control specialists to append a NOTAM onto the digitized voice output for the local weather observation message. The printer provides hard copy data output of weather summaries, routine METAR's, SPECI's, and log messages. Log messages identify system status. The system maintenance log provides the technician with the maintenance history of the system and provides the results of each self-test performed on the system. If an SCA unit fails self-test, the log records the source of failure.

14.4.9 MODEMS

Three categories of modems provide I/O interfaces: phone line, dedicated line (for stand-alone modems), and rf. Table 14.4.3 lists the complement of standard and optional modems available in the SCA. All sites are equipped with data communication for one user via stand-alone modem. A second user can be accommodated by an additional (optional) 2400 baud or 28800 baud stand-alone modem.

14.4.9.1 **Telephone Modems.** The SCA contains up to six telephone modems which provide communications to external devices over leased lines or public, switched-telephone networks. All data transfers are under the control of the SIO boards that communicate with data terminal equipment (DTE) ports of those modems which use RS-232 protocol. The telephone modems operate in a 2-wire, full-duplex mode. These modems operate at data rates of 2400, 9600, or 28800 baud.

Modems available for the single-cabinet ASOS are listed in table 14.4.3. These additional modems can be installed, as required, to provide the connections to AFOS phone, proximity user OID, ADAS, or other user requirements.

14.4.9.2 **RF Modems.** The rf modems are used by the SCA for intercabinet communications at sites equipped with DCP's. The rf modems operate in the UHF range through an omnidirectional antenna or Yagi antenna (used in conjunction with 3 dB, 6 dB, 10 dB, 20dB, or 30 dB attenuators at sites where co-channel interference exists). A second, redundant, rf modem can be added, together with RF Switch 7A1A1A5S1. The rf switch (DPST coaxial relay) is installed at all sites where two rf modems are used. The rf switch connects the active rf modem to the antenna. The rf switch is controlled by the CPU via DIO board A15. When the CPU senses a failure in the rf modem communications link, it writes a selection word to the DIO board to toggle the switch. The CPU communicates with modem RF #1 through SIO board #2 and with RF #2 through SIO board #3.

\$
\$
\$

Table 14.4.3. Modem Complement

Ref Des	Modem #	Category	Function/Type	CAGE	Model/PN
7A1A1A5A1*	RF #1	RF	DCP Communications		90315-10 or -20
7A1A1A5A2*	RF #2	RF	DCP Communications		90315-10 or -20
7A1A1A9	User #1	Stand-alone	User #1, 2400 Baud	97384	90051-1
7A1A1A10*	User #2	Stand-alone	User #2, 2400 Baud or 28800 Baud	97384	90051-1 or 90431-1
7A1A1A11*	#3	Telephone line	2400 or 9600 Baud	97384	90050-1, 90051-1
7A1A1A12*	#4	Telephone line	2400 or 9600 Baud	97384	90050-1, 90051-1
7A1A5*	#5	(Optional category & use.)			
7A1A6*	#6	(Optional category & use.)			
7A2A1A1*		Stand-alone	Codex Modem	97384	90362-10 or -20

\$
\$

* Optional