

SECTION IV. THEORY OF OPERATION

2.4.1 ACU AND PERIPHERALS OVERVIEW

The task of central control and dissemination of all data is performed by the acquisition control unit (ACU), which is the central receiving point of all sensor data. The ACU receives sensor data from the data collection packages (DCP's), processes the data according to preprogrammed instructions (algorithms), and outputs the appropriate information to the various peripheral devices and users. In addition, the ACU controls a speech processor that communicates using digitized human speech. Another important feature of the ACU is the conduct of all diagnostic routines and the meaningful interpretation of results to maintenance personnel. This section describes ACU theory of operation at the simplified block diagram and detailed block diagram levels. The Codex modem, when furnished, is described in Chapter 13.

2.4.2 SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the ACU is depicted on figure 2.4.1. The major subassemblies of the ACU are the card rack assembly, the modem ac power rack, the power supply assembly, the dc power supply enclosure, the rf/pressure mounting shelf, the I/O panel assembly, and the battery box. The ACU's major functions are grouped into three functional areas: data processing, data input/output, and power distribution and control. These functional areas are discussed in the following paragraphs.

2.4.2.1 Data Processing. The data processing functional area is responsible for system timing and control, data processing, data formatting and storage, and data quality checks. All hardware required for data processing is contained in the card rack assembly and includes two central processing units (CPU's) and a memory board.

2.4.2.1.1 Central Processing Units (CPU's). The CPU boards provide central processing and control for the entire ASOS. Both CPU boards are identical. The CPU boards are programmed to perform self-tests once per second during real-time operation and constantly monitor each other. If a self-test error is detected, the faulty CPU is flagged off-line and the other CPU assumes the processing duties.

2.4.2.1.2 Memory Board. The memory board contains the ASOS operational software used by the CPU's. The memory board also stores archive data, the maintenance log, and site specific constants. The board contains up to 6 megabytes of memory with a battery backup for random access memory (RAM) in the event of a power failure.

2.4.2.2 Data Input/Output. The data input/output (I/O) functional area is responsible for data acquisition and communications between the data processing functional area and the ASOS users (Chapter 1). Due to the large number and variety of ASOS communications, the I/O functional area is the largest and most complex of the ACU system. Communications between ASOS users and the data processing functional area are established through telephone lines, modems, and I/O boards. Communications between the ACU and DCP are established through I/O boards and rf modems (or optional line drivers). Communications between the pressure sensors and the data processing functional area are established through I/O boards. Five different types of I/O boards exist: serial I/O, analog to digital (A/D), digital I/O, digital voice processing, and video controller. The type of I/O board used is dependent on the requirements of the user. The modems (up to 10) contained in the modem ac power rack are used for remote communications via telephone lines. The rf/pressure mounting shelf contains up to two rf modems (primary and secondary). The rf modems are used to establish an rf communications link between the ACU and the DCP's when no direct lines are available. When direct lines are available at the DCP, communications are accomplished through line drivers (short

haul modems) located in the modem ac power rack. ACU I/O hardware is described in the following paragraphs.

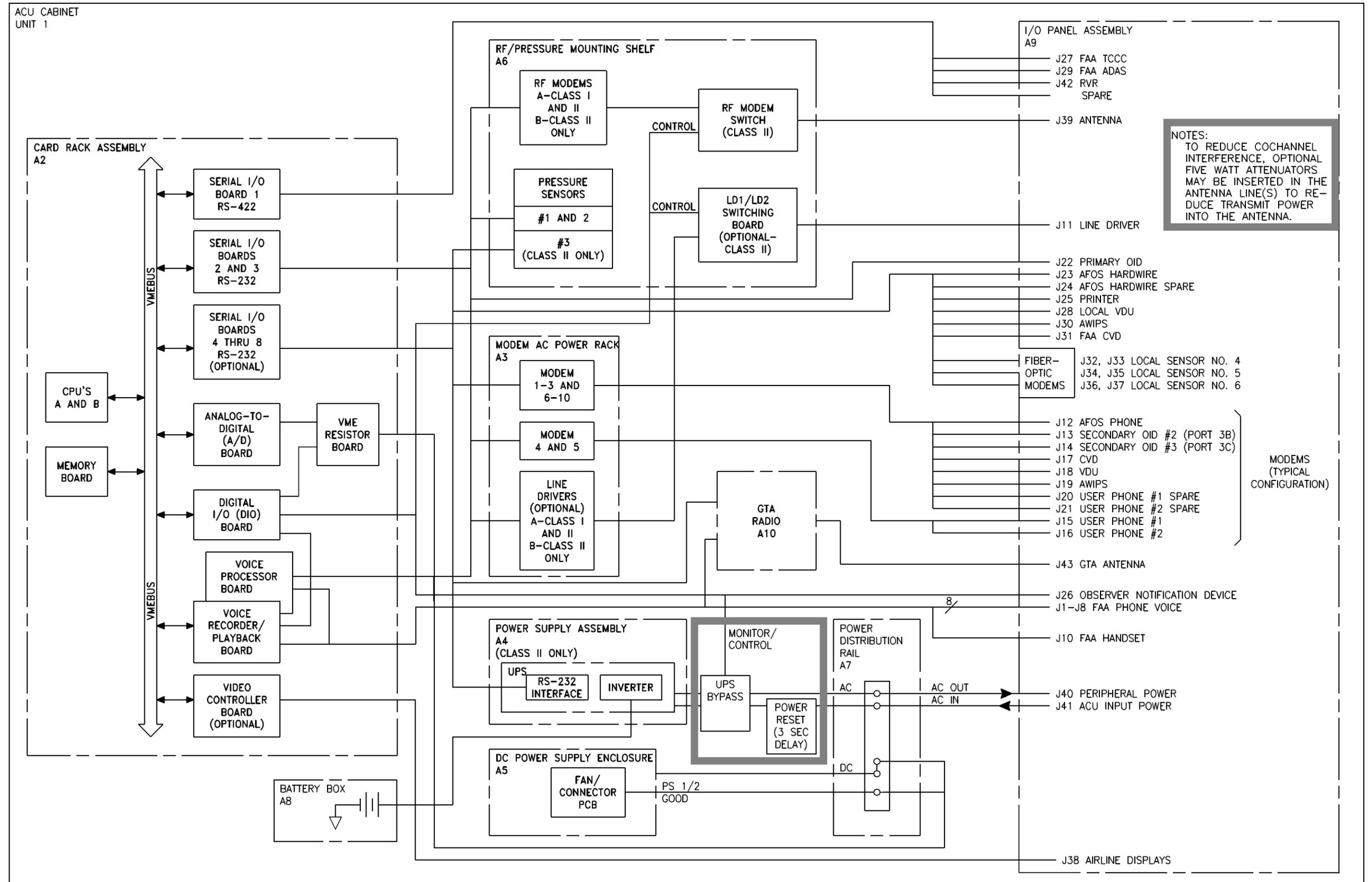
2.4.2.2.1 Serial I/O Boards. From three to eight serial I/O (SIO) boards are used to interface the ACU CPU boards with other communications equipment. SIO board 1 is a model XVME 401 interface, which provides four RS-422 serial I/O ports. SIO board 1 is dedicated to the FAA tower computer control complex (TCCC), the FAA ADAS, and RVR. All other SIO boards are model XVME 490/1, each of which provides four RS-232 ports. SIO boards 2 and 3 are dedicated to the two (in Class II) rf modems or line drivers, the first two pressure sensors, modems 4 and 5 in the modem ac power rack (these correspond to user phone 1 and 2 ports), the digital voice system, and the primary operator interface device (OID). SIO boards 4 through 8 are optional. Unlike the first three SIO boards, their individual I/O ports are not dedicated to specific pieces of equipment. Rather, their ports are assigned to various equipments by the ACU serial communications page on the OID. They may interface any piece of equipment requiring RS-232 communications, such as the printer, a local video display unit (VDU), a controller video display (CVD), AFOS hardwire and spare, or the other modems in the modem ac power rack, etc.

2.4.2.2.2 Analog to Digital (A/D) and VME Resistor Boards. The A/D board converts analog signals to digital data so that the data can be read by the CPU. These boards convert analog dc power monitor signals from the dc power supplies and the rf modems into digital data. The CPU then reads the data to determine the power status of the dc power supplies and the rf modems. The VME resistor board scales the dc voltages before they are applied to the A/D board.

2.4.2.2.3 Digital I/O Board. The digital I/O board contains four digital I/O ports that allow the CPU to read and write control signals from and to the ACU. In particular, the digital I/O board inputs status signals from the dc power supplies and the voice processor board (via the VME resistor board). In Class II systems, the digital I/O board outputs a control signal to control an rf modem switch (or line driver relay) that switches between the primary and secondary rf modems (or line driver). The digital I/O board in the Class II system also monitors and controls the UPS bypass circuit.

2.4.2.2.4 Digital Voice Processing. Digital voice processing consists of three operations: producing a verbal report from a stored vocabulary based on current ASOS data, recording an operator-generated addendum up to 90 seconds long, and producing an output consisting of the automatically generated data and the operator input. Outputs are available for the FAA handset, dial-up reports, and FAA radio communications for aircraft. Voice processing is accomplished with two dedicated boards: a voice processor board and a voice recorder/playback board. The voice processor board contains the CPU for the digital voice system. It receives digital voice files from the ASOS CPU, creates voice reports consistent with the data reported by the sensors, and receives operator-generated digitized audio from the voice recorder/playback board. The voice recorder/playback board receives digitized voice from the voice processor board and converts the data into audio. Audio is output for dial-in weather requests, for the FAA handset at OID port 5C, and to the GTA radio for pilot use. In addition, the voice recorder/playback board receives input voice audio from the FAA handset, digitizes the input audio, and transfers the digitized audio to the voice processor board for storage in RAM.

2.4.2.2.5 Video Controller Board. The video controller board is an option that can be installed in the ACU to allow it to drive external airline displays that are not part of the ASOS. The video controller board outputs a composite RS-170 video signal required to drive the airline video displays.



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Figure 2.4.1. ACU Simplified Block Diagram

2.4.2.2.6 ACU/DCP Communication. Communications between the ACU and DCP are established via an rf modem or line driver link. For Class II systems using an rf modem link, the communication system consists of two rf modems, an rf modem switch, and an rf antenna. The CPU communicates with one of the modems via an SIO board RS-232 data link. The modem, in turn, communicates with the DCP via the rf antenna. The two rf modems are identical, with one serving as the primary communications link and the other as a backup. The rf switch selects which modem uses the antenna. In the event that the primary rf modem fails (transmitter or receiver), all communications are automatically switched to the secondary rf modem. For Class I systems, a single rf modem provides the data link (rf switch is not required). The line driver communication link is similar, except that communication with the DCP is over a direct line rather than the airwaves. For Class II systems, two line drivers are installed in the modem ac power rack, and an LD1/LD2 switching board (installed in the rf/pressure mounting shelf) switches between primary and secondary line drivers. For Class I systems, a single line driver handles all ACU/DCP communication.

2.4.2.2.7 Telephone Modems. Telephone modems are used to provide communication between the ACU and remote users or other devices (refer to Chapter 1, Section I for a list of the ASOS users who can receive/transmit data over modems). The modem ac power rack can contain up to 10 modems. Three different models may be installed in the modem rack: model 2440 (2400 baud), model V.3225 (9600 baud), and model V.3400 (28800 baud). The model 2440 modem is used for USER PHONE #1 (modem 4, refer to figure 2.1.4), USER PHONE #2 (at some sites), and most other applications. The model V.3225 is used with optional OID #2 (port 3B) and optional OID #3 (port 3C). The model V.3400 is used for USER PHONE #2 instead of the model 2440 at selected sites.

Modems 4 and 5 are included in every installation and are dedicated to the USER PHONE #1 and #2 communication ports. These two modems communicate with the CPU via specific ports on SIO boards 2 and 3, respectively. All of the other modems are provided as needed for communications options. These modems may be connected to any port on SIO boards 4 through 8, depending upon how the ACU communications are configured on the ACU serial communications page of the OID.

2.4.2.3 Power Distribution and Control. The power distribution and control functional area consists of Power Distribution Rail A7, DC Power Supply Enclosure A5, and Power Supply Assembly A4 (Class II systems only). The power distribution rail consists of a terminal strip that distributes ac and dc power and a power reset relay that delays power application to the ACU for three seconds after site power is interrupted. The dc power supply enclosure contains two identical power supplies that generate +5 volts, -12 volts, and +12 volts. These two power supplies are wired in parallel to provide a guaranteed output in the event that either supply fails. Special circuits built into the power supplies prevent a failed power supply from dragging down the operational power supply. Class II systems contain an uninterruptible power supply (UPS) bypass circuit mounted on Power Distribution Rail A7. The UPS bypass circuit provides additional power source control and monitoring. In the event of a power failure, the UPS is capable of supplying backup ac power to the ACU under full load for a minimum of 10 minutes. Special line loss circuitry in the UPS constantly monitors the input voltage for a power loss. When a power loss is detected, the circuitry allows Battery Box A8 to drive an inverter (dc to ac conversion), which supplies ac power to the ACU. ACU components requiring ac power are the dc power supplies and the modem ac power rack. The primary OID, the printer, and the FAA modems also receive UPS backup power via PERIPHERAL POWER connector J40 on the I/O panel assembly. Any additional peripherals connected to the UPS place an extra load on the UPS and reduce its capability to supply power. The UPS and Battery Box A8 are not included in Class I systems. For these systems, ac power for internal ACU equipment and the PERIPHERAL POWER connection is supplied directly from the input power applied to ACU INPUT POWER connector J41.

2.4.3 DETAILED BLOCK DIAGRAM DESCRIPTION

2.4.3.1 General. This section contains descriptions and detailed block diagrams of the ASOS ACU. The card rack assembly is described using a detailed block diagram. The circuit cards dedicated to processing ASOS sensor data are also described. Descriptions of the rf and telephone modems, digital pressure sensors, and local sensor fiber optic modems include theory of operation and associated diagrams.

Peripherals associated with the ACU, and connected through the connector panel, are the printer, CVD's, VDU's, OID's, airline displays, OND, and FAA handset. Repair of a faulty ACU peripheral consists of replacing the failed peripheral. Accordingly, the theory of operation of peripherals is presented on a general level. The drawings associated with peripherals are intended to provide the technician with the information necessary to conduct continuity checks when a connector is suspected of being faulty or needs replacement. Power distribution and control is described using detailed block diagrams of the distribution of dc and ac voltages to the ACU, including the UPS in the power supply assembly.

2.4.3.2 Card Rack Assembly. The card rack assembly contains up to 17 circuit boards that perform all of the data processing and input/output functions. The following circuit boards are used specifically to process data: CPU's A and B, and the memory board provide the computational system for the ACU. The following circuit boards perform the ACU input/output functions: serial I/O (SIO) boards (up to eight), the A/D board (in conjunction with the VME resistor board), the digital I/O board, the voice processor and voice recorder/playback boards, and the video controller board. All of the circuit boards are designed to accommodate the VMEbus backplane construction. Figure 2.4.2 illustrates the VMEbus chassis, backplane configuration, and connector pin assignments as required by the VMEbus specification. One or two 96-pin bus connectors are located on the rear edge of the board and are labeled P1 and P2. The 96-pin connectors consist of 3 rows of pins (32 pins per row) labeled rows A, B, and C. The pin connections for P1 contain the standard address, data, and control signals necessary for system bus communication. The P1 pin assignments are listed by pin number order. The pin connections for P2 vary according to the function provided by the circuit board. The following paragraphs provide detailed information on the circuit boards and their dedicated functions, and reference figure 2.4.3 (ACU Card Rack Assembly Detailed Block Diagram).

2.4.3.2.1 Central Processing Unit (CPU). The CPU executes the ASOS operational software. All operational software resides in the erasable programmable read-only memory (EPROM) on the memory board. Execution of the operational software involves data processing, data formatting, data quality checks, and data storage. The card rack assembly contains two CPU circuit boards, both of which are identical and contain a 68010 series microprocessor running at 10 MHZ, memory (EPROM and dynamic random access memory (DRAM)), two RS-232 ports, and a 16-bit timer. During system operation, one of the CPU's functions as the primary CPU, which performs all processing and I/O functions. The other (secondary) CPU provides a redundant processor. If, at any time, the primary CPU fails, it is taken off-line and the secondary CPU becomes the primary CPU. Initially, CPU A is the primary CPU. Two pushbutton switches labeled RESET and ABORT are provided on the front of the circuit board. ABORT halts program execution without resetting the CPU. This switch is used for development purposes and should not be used in the field. In the event that ABORT is pressed, RESET should be pressed to reset the CPU and activate SYSRESET, thereby resetting the entire backplane via the VMEbus. Resetting the CPU does not affect the contents of the DRAM. The following paragraphs provide a detailed block diagram description of the CPU and its various modes of operation.

The CPU consists of nine functional areas (Figure 2.4.3): the system resource function, dual UART and timer, RS-232 driver and receiver logic, CPU clock, CPU, interrupt logic, VME interface logic, address buffer and decode, and memory. The system resource function on CPU A provides the system clock, system reset, bus arbitration, and bus timer functions for the entire VMEbus. Because CPU A is the bus controller, the system resource function on CPU B is not used.

The dual UART and timer provides two RS-232 serial communication channels (channels A and B), a timer, and two I/O and control ports. The RS-232 driver and receiver logic interfaces UART channels A and B to external devices via connector JK1 on the CPU by providing standard transmit and receive lines. On both CPU A and CPU B, the two channels are not used. On CPU A, however, a loopback jumper is

P1 (VME BUS) PIN ASSIGNMENTS

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY	D08
2	D01	BCLR	D09
3	D02	ACFAIL	D10
4	D03	BG0IN	D11
5	D04	BG0OUT	D12
6	D05	BG1IN	D13
7	D06	BG1OUT	D14
8	D07	BG2IN	D15
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	SYSFAIL
11	GND	BG3OUT	BERR
12	DS1	BR0	SYSRESET
13	DS0	BR1	LWORD
14	WRITE	BR2	AM5
15	GND	BR3	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN	SERCLK(1)	A17
22	IACKOUT	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7	A14
25	A06	IRQ6	A13
26	A05	IRQ5	A12
27	A04	IRQ4	A11
28	A03	IRQ3	A10
29	A02	IRQ2	A09
30	A01	IRQ1	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

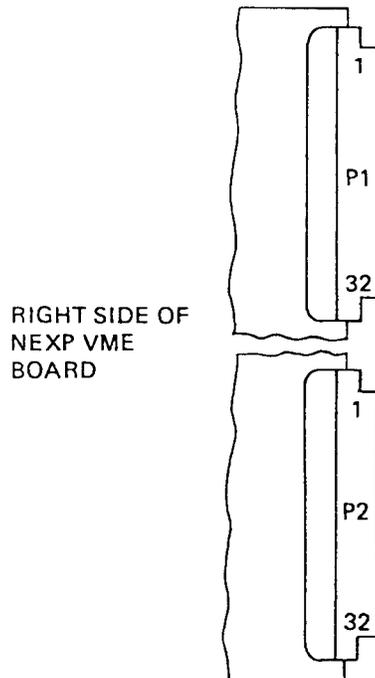


Figure 2.4.2. ACU VMEbus Chassis and Connector Pin Assignments (Sheet 1 of 3)

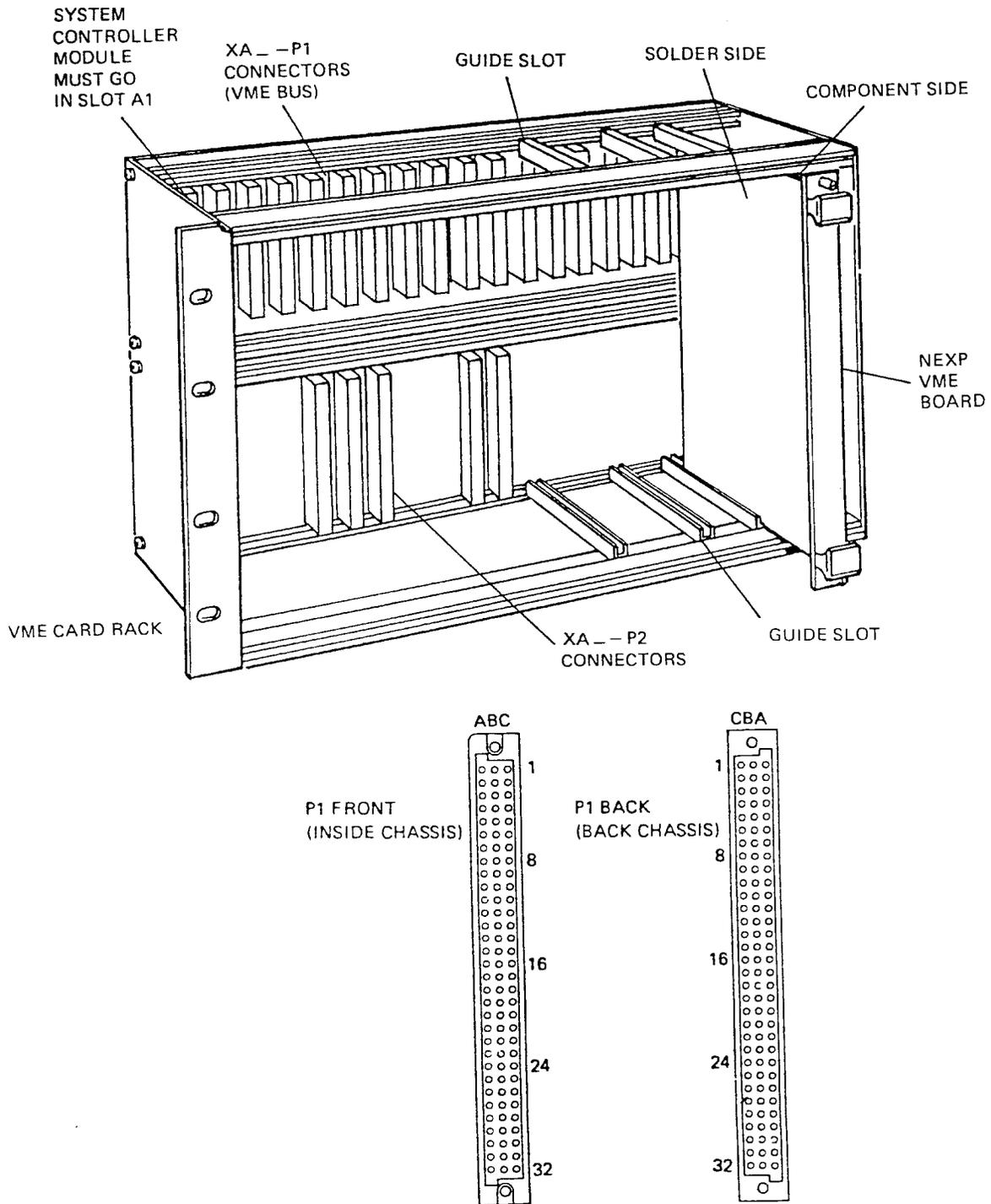


Figure 2.4.2. ACU VMEbus Chassis and Connector Pin Assignments (Sheet 2)

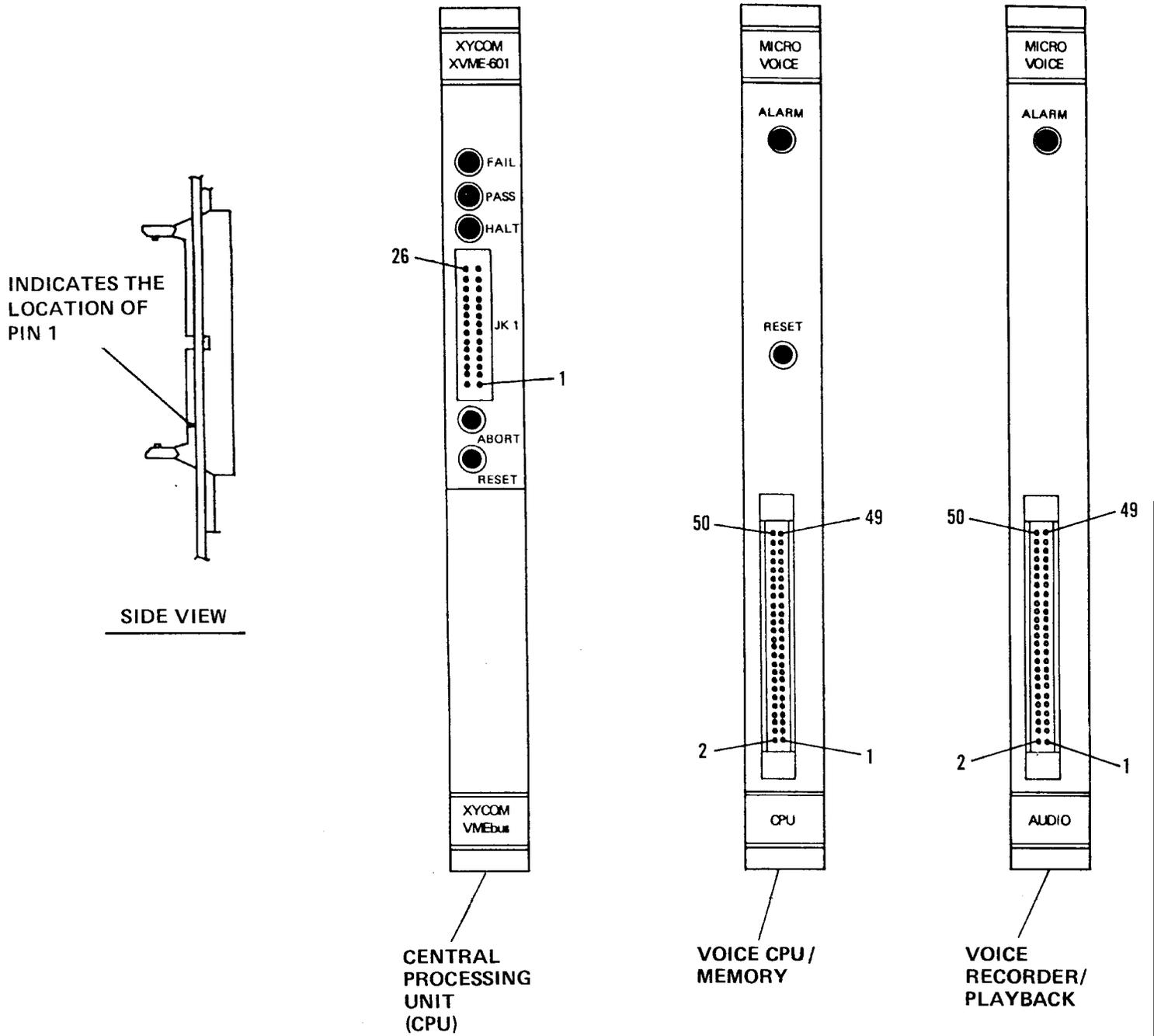


Figure 2.4.2. ACU VMEbus Chassis and Connector Pin Assignments (Sheet 3)
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installed between the channel B transmit and receive lines (pins 14 and 16 of connector JK1). This jumper identifies CPU A as the initial primary CPU. When power is first applied to the ACU, both CPU's issue a message from their respective UART channel B. CPU A then receives the message back via the installed loopback jumper. Both CPU's then examine their receive lines. When CPU A detects that it has received the signal via the loopback jumper, it assumes the role of the primary CPU. When CPU B detects that it has not received its transmitted signal, it assumes the role of the secondary CPU. The secondary CPU continuously monitors the primary CPU status by examining a memory location in the memory board used to store a free running count. The primary CPU updates this count on a periodic basis. Failure to update the count indicates a CPU failure. The secondary CPU then becomes the primary CPU.

The CPU clock provides the 10 MHZ clock signal required by the CPU. The CPU executes the ASOS operational software. The interrupt logic monitors the dedicated interrupt lines and informs the CPU when an interrupt line is active. The interrupts are prioritized and processed on a first come, first serve basis. The VME interface logic provides the standard address, data, and control signals necessary for system bus communication. The address buffer and decode provides the address. The onboard memory consists of 128K bytes of EPROM and 512K bytes of DRAM. The operating system software for the CPU is contained in the EPROM. The refresh circuitry for the DRAM is not disabled during a RESET; therefore, the CPU may be reset without affecting the memory contents.

The ACU continuous self-test (CST) checks the status of the CPU's once per minute. CST results are displayed on the CPU page of the OID. The CST checks the following areas of both the primary and secondary CPU: DRAM, EPROM, BUS ERRORS, SERIAL PORT #1 and #2 LOOPBACK, and SERIAL PORT #1 and #2 XMIT ERRORS. For the primary CPU, test pass/fail status is displayed for each of these areas. For the secondary (redundant) CPU, test status is displayed for the overall board only. The technician can manually run the CPU test from the CPU page at any time. A T status is displayed for each test category until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The DRAM test is based on an alternating pattern. Data are output to the DRAM and read back, the returned data are evaluated, and the test status is displayed. The EPROM test is based on a checksum. The checksum is compared to the last byte in the EPROM, the result is evaluated, and the test status is displayed. The BUS ERRORS test is based on a memory write to a specific address, with the contents of the addressed memory evaluated and the test status displayed.

The SERIAL PORT #1 and #2 LOOPBACK tests ensure that the CPU can communicate with its internal UART. The CPU reads the UART interrupt vector register and checks for bus errors. Test status is displayed as P (pass) if no bus errors occurred.

For the SERIAL PORT #1 and #2 XMIT ERRORS test, the CPU reads the contents of the status register for the corresponding port. This register contains information on transmission errors detected by the UART during RS-232 communications. Specifically, the CPU checks the status register for parity errors, framing errors, and overrun errors that may have occurred. If such errors occur for three consecutive CST cycles, an F (fail) is displayed for the test status; otherwise, test status is P (pass).

2.4.3.2.2 Memory Board. The XVME-110 memory board contains three memory banks. Each bank is independently configured via jumpers to specify VME address/memory chip size, device speed, device pinout, and backup power. The following paragraphs provide a detailed block diagram description of the memory board.

The memory board consists of nine functional areas (Figure 2.4.3): banks 1, 2, and 3 memory devices; VME/bank address decode and control; battery backup; data buffer; bus cycle control; address buffer and decode logic; and the system real-time clock. The first bank contains up to 4 Mbytes of EPROM. The EPROM contains the operational software program run by the CPU. It also contains the DCP software load that is transferred to a DCP in the event that a DCP loses its program load and requires reinitialization. Banks

2 and 3 contain up to 2 Mbytes of static random access memory (SRAM). The SRAM provides storage for ASOS weather archives. The address and control signals used to address memory locations are generated by the VME/bank address decode and control. The memory boards are configured with a battery backup to provide an alternate power source in the event of a power loss. The data buffer, bus cycle control, and address buffer and decode logic provide the standard address, data, and control signals necessary for system bus communication. The real-time clock maintains clock calendar timing, which is accessed by the CPU upon initialization. When initialized, the CPU maintains a clock via software.

The ACU continuous self-test (CST) checks the status of the memory board once per minute. CST results are displayed on the memory page of the OID. The CST performs an EPROM test and an SRAM test. The technician can manually run the memory test from the memory page at any time. A T status is displayed for each test category until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The EPROM test is based on a checksum, which is compared to the last byte in the EPROM. The result is evaluated and the test status is displayed. The SRAM test ensures that the CPU can read data from the SRAM on the memory board without encountering bus errors.

2.4.3.2.3 Serial I/O (SIO) Board. The card rack assembly contains one XVME-491 SIO board and up to seven XVME-490/1 SIO boards. The XVME-491/1 SIO board (SIO board 1) provides four RS-422 serial ports, while each of the XVME-490/1 SIO boards (SIO boards 2 through 8) provides four RS-232 ports. The SIO boards communicate with the CPU on a character-by-character basis. The CPU must process interrupts on each and every transmitted and received character. The following paragraphs provide a detailed block diagram description of the SIO board.

The SIO board consists of six functional areas (Figure 2.4.4): two serial communication controllers (SCC's), interrupt logic, data buffer, bus cycle control, and address buffer and decode logic. The SCC's provide a variety of communication modes. Upon power up, the CPU initializes the SCC's to the proper communication modes. Interrupts are generated via the interrupt logic. An interrupt can signify that a received character is available, that the transmit buffer is empty, or an external/ status change. The data buffer, bus cycle control, and address buffer and decode logic provide the standard address, data, and control signals necessary for system bus communication.

The four ports of each of SIO boards 1 through 3 are factory assigned to specific devices. Their ports are dedicated to these devices via corresponding connectors on the ACU main wiring harness. Although these ports can be reassigned via the ACU serial communications page of the OID, the technician should not reassign them; assigning these ports to other FRU's would invalidate their corresponding harness markers. Table 2.4.1 identifies each of the ports of these SIO boards and lists the corresponding harness connector and the device to which it is connected.

Unlike SIO boards 1 through 3, SIO boards 4 through 8 are optional. Most systems will not have all of these SIO boards installed. As such, the ports of these SIO boards are not factory assigned to specific devices. Rather, these ports are assigned to various devices during the initial configuration of the system. This assignment is made via the ACU serial communications page of the OID. Figure 2.4.4 identifies all of the ports of SIO boards 4 through 8 and identifies the W014 (or W016) connector that corresponds to each. The devices to which these connectors mate depend upon the device assigned to that port by the ACU serial communications page. Figure 2.4.4 also identifies the pin-to-pin wiring between each of the SIO boards and their respective connectors.

Table 2.4.1. Port Assignments for SIO's 1 Through 3

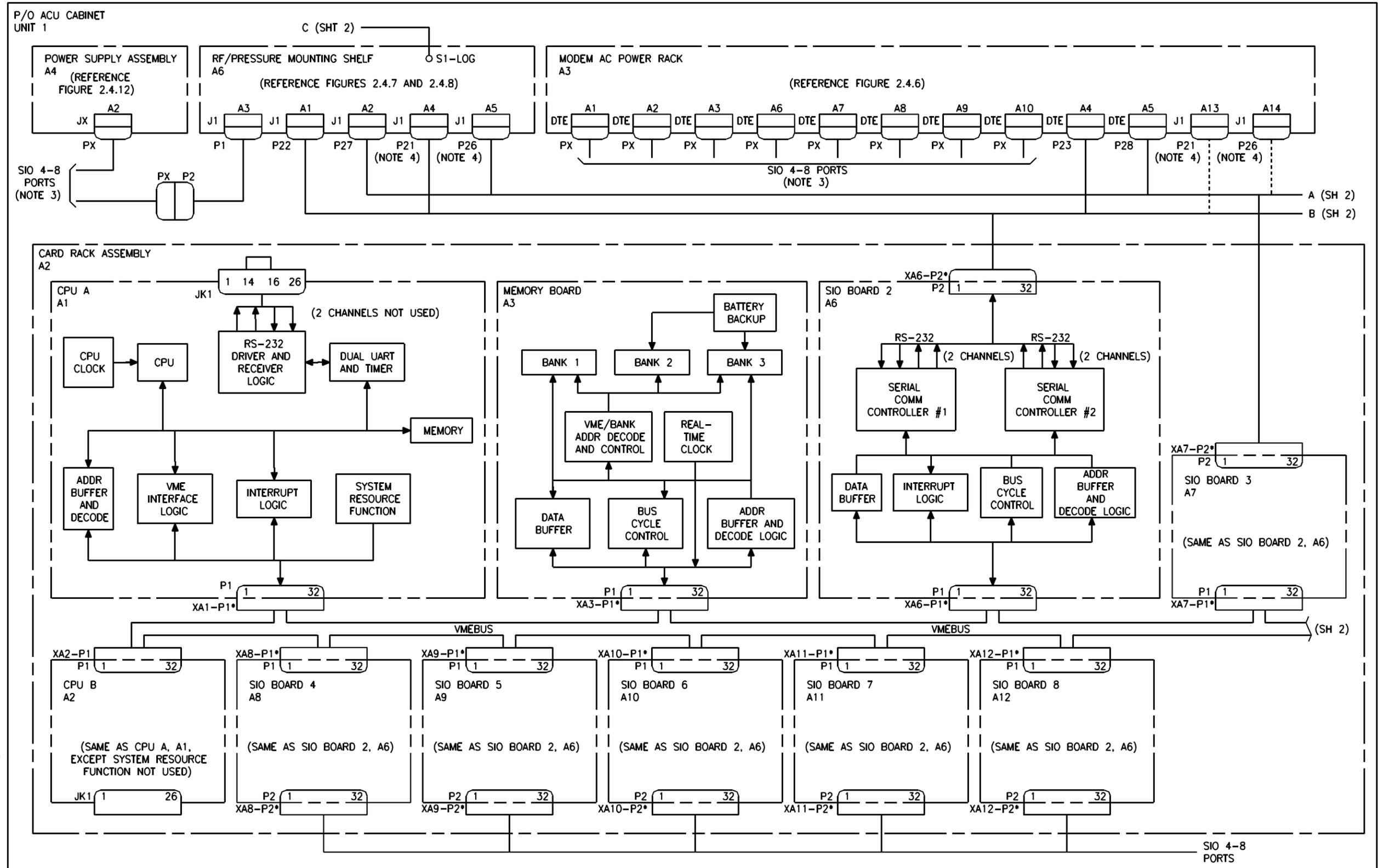
SIO Board	Port	W014/16 Connector	Device	Function
1 (RS-422) Note 1	1	P16	1A9J29	FAA ADAS
	2	P17	1A9J27	FAA TCCC
	3	P18	1A9J42	RVR
	4	P19	N/A	Spare
2 (RS-232)	1	P21	1A6A4 or 1A3A13	RF Modem A Line Driver A
	2	P22	A6A1	Pressure Sensor #1
	3	P23	1A3A4	Modem #4 (User Phone #1)
	4	XA20-P2	1A2A20	Voice Processor Board
3 (RS-232)	1	P26	1A6A5 or 1A3A14	RF Modem B (Class II only) Line Driver B (Class II only)
	2	P27	1A6A2	Pressure Sensor #2
	3	P28	1A3A5	Modem #5 (User Phone #2)
	4	P29	1A9J22	Primary OID

Note 1- ACU S/N 288 and below use crossover connector cables (W77) between W014/16 and the device connectors to configure the RS-422 ports for DTE I/O. ACU S/N 289 and above are factory wired for DTE I/O.

The ACU CST checks the status of the SIO boards once per minute. CST results are displayed on the ACU SIO display pages of the OID (there is one page for each of the eight SIO boards). The CST performs a LOOPBACK test and an XMIT ERRORS test on each of the four ports of an SIO board. The technician can manually run the SIO test from an SIO page at any time. A T status is displayed for both test categories until the test is run again during the next CTS cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

For the LOOPBACK test, the CPU reads an interrupt vector register on the SIO board to ensure that it can communicate with the SIO port. For the XMIT ERRORS test, the CPU reads the contents of the SCC status register for the corresponding port. This register contains information on transmission errors detected by the SCC during RS-232 communications. Specifically, the CPU checks the status register for parity errors, framing errors, and overrun errors that may have occurred. For both LOOPBACK and XMIT ERRORS tests, CST status is displayed as either P (pass), F (fail), or D (degraded). A status of D is displayed if five or more errors have been detected and the port is currently passing the test. At 0600 LST each day, the number of accumulated failures is summarized in the system (maintenance) log. Paragraph 1.3.4.3.3 provides additional information on SIO test reporting.

2.4.3.2.4 Voice Processor and Voice Recorder/Playback Boards. The voice processor board and the voice recorder/playback board make up the digital voice processing system of the ACU. Both of these boards are connected to the VMEbus for power and system reset purposes. Communication between the CPU and the digital voice system is accomplished via the RS-232 link between SIO board 2 and the voice processor board (rather than over the VMEbus). The voice processor board communicates with the voice recorder/playback board via a 50-pin ribbon cable connected between the front panels of both boards. Voice outputs from the digital voice system are passed to the I/O panel where they are made available for dial-up reports, the FAA handset, and FAA radio communications for aircraft. Additional information on these boards is provided in the digital voice processor detailed block diagram description (paragraph 2.4.3.3).



- NOTES
- UNLESS OTHERWISE NOTED, ALL ACU CABINET WIRING IS PART OF HARNESS WO14 (CLASS II) OR WO16 (CLASS I).
 - REFERENCE FIGURE 2.4.2 FOR ACU VMEBUS CHASSIS AND PIN ASSIGNMENTS.
 - WO14/WO16 CONNECTOR (PX) ATTACHED TO FRU DEPENDS UPON WHICH SIO PORT THE FRU IS ASSIGNED (VIA ACU SERIAL COMMS DISPLAY ON OI). REFER TO FIGURE 2.4.4 FOR SIO PORT-TO-PX RELATIONSHIP.
 - WO14/WO16 CONNECTORS P21 AND P26 GO TO EITHER RF MODEMS OR LINE DRIVERS, DEPENDING ON SITE CONFIGURATION.

Figure 2.4.3. ACU Card Rack Assembly Detailed Block Diagram (Sheet 1 of 2)

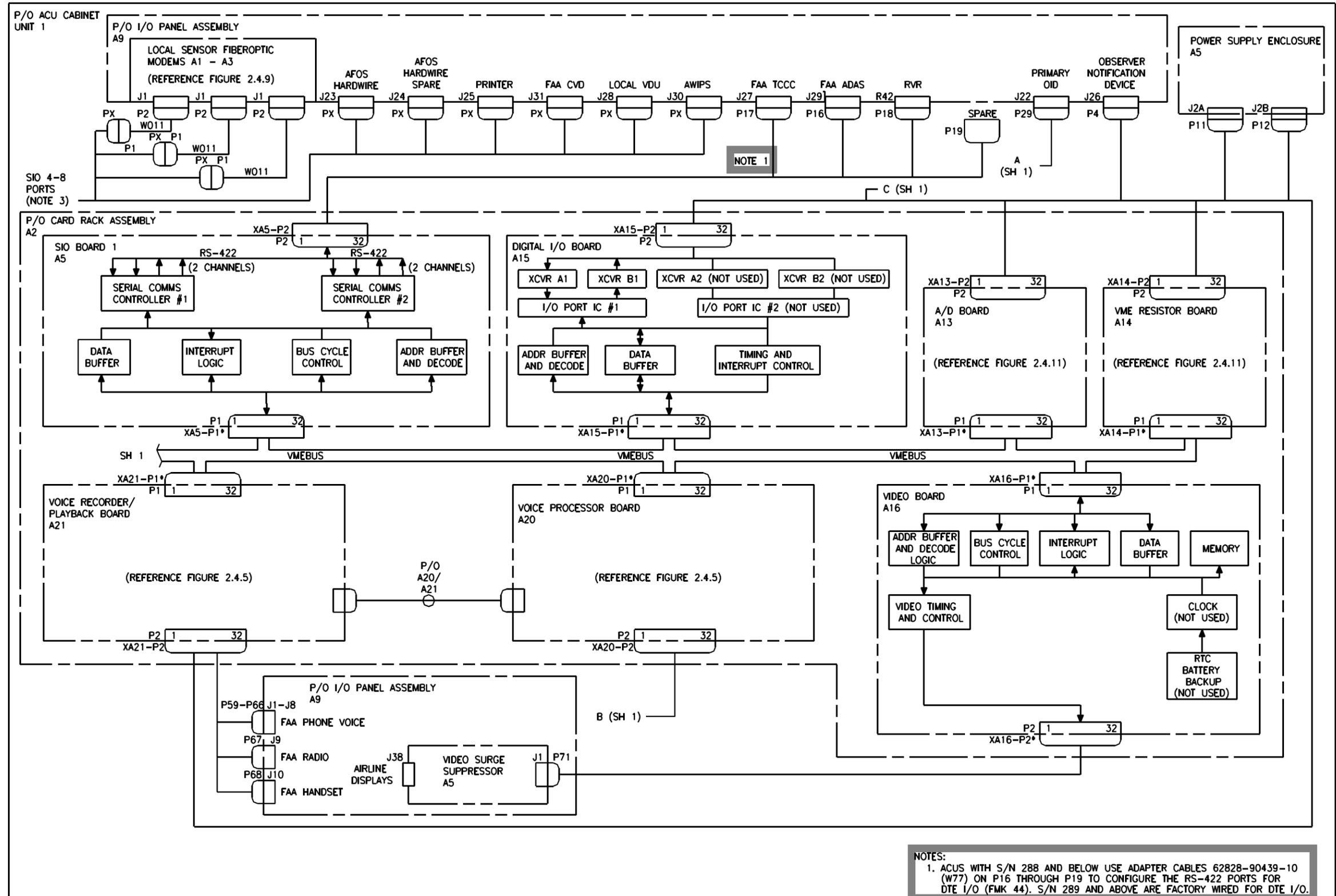
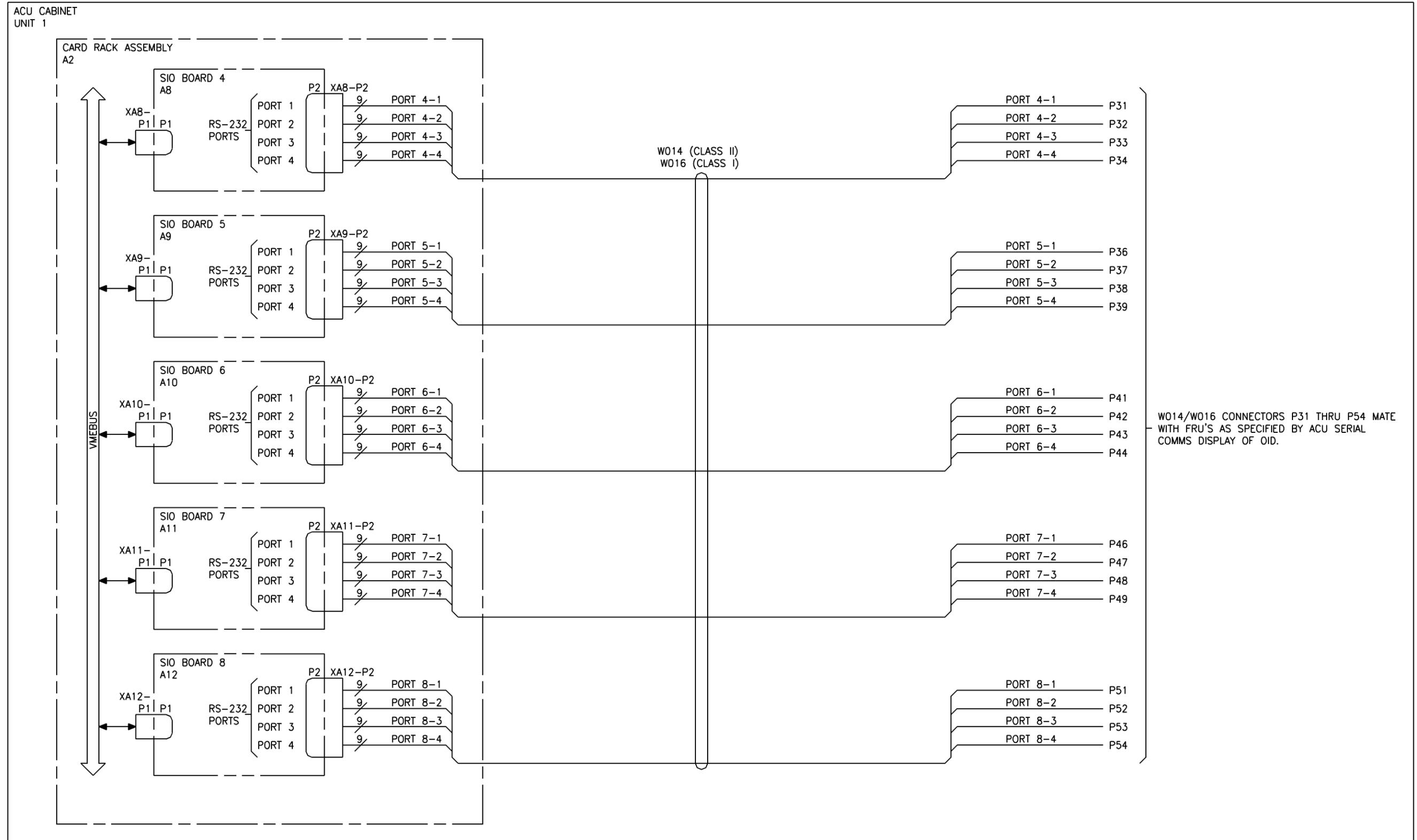


Figure 2.4.3. ACU Card Rack Assembly Detailed Block Diagram (Sheet 2)



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Figure 2.4.4. SIO Boards 4 Through 8 Ports and Pin Assignments (Sheet 1 of 2)

SIO BOARDS 4-8 TO W014/W016 CONNECTOR (PX) PIN ASSIGNMENTS

	SIO BOARD 4 (1A2A8)			SIO BOARD 5 (1A2A9)			SIO BOARD 6 (1A2A10)			SIO BOARD 7 (1A2A11)			SIO BOARD 8 (1A2A12)		
	FROM	TO	SIGNAL	FROM	TO	SIGNAL	FROM	TO	SIGNAL	FROM	TO	SIGNAL	FROM	TO	SIGNAL
PORT 1	A2XA8P2-A4	P31-17	RXC0	A2XA9P2-A4	P36-17	RXC0	A2XA10P2-A4	P41-17	RXC0	A2XA11P2-A4	P46-17	RXC0	A2XA12P2-A4	P51-17	RXC0
	A2XA8P2-A1	P31-2	TXD0	A2XA9P2-A1	P36-2	TXD0	A2XA10P2-A1	P41-2	TXD0	A2XA11P2-A1	P46-2	TXD0	A2XA12P2-A1	P51-2	TXD0
	A2XA8P2-A6	P31-20	DTR0	A2XA9P2-A6	P36-20	DTR0	A2XA10P2-A6	P41-20	DTR0	A2XA11P2-A6	P46-20	DTR0	A2XA12P2-A6	P51-20	DTR0
	A2XA8P2-A8	P31-24	TXC0	A2XA9P2-A8	P36-24	TXC0	A2XA10P2-A8	P41-24	TXC0	A2XA11P2-A8	P46-24	TXC0	A2XA12P2-A8	P51-24	TXC0
	A2XA8P2-A2	P31-3	RXD0	A2XA9P2-A2	P36-3	RXD0	A2XA10P2-A2	P41-3	RXD0	A2XA11P2-A2	P46-3	RXD0	A2XA12P2-A2	P51-3	RXD0
	A2XA8P2-A3	P31-4	RTS0	A2XA9P2-A3	P36-4	RTS0	A2XA10P2-A3	P41-4	RTS0	A2XA11P2-A3	P46-4	RTS0	A2XA12P2-A3	P51-4	RTS0
	A2XA8P2-A5	P31-5	CTS0	A2XA9P2-A5	P36-5	CTS0	A2XA10P2-A5	P41-5	CTS0	A2XA11P2-A5	P46-5	CTS0	A2XA12P2-A5	P51-5	CTS0
	A2XA8P2-C1	P31-7	GNDO	A2XA9P2-C1	P36-7	GNDO	A2XA10P2-C1	P41-7	GNDO	A2XA11P2-C1	P46-7	GNDO	A2XA12P2-C1	P51-7	GNDO
A2XA8P2-A7	P31-8	DCD0	A2XA9P2-A7	P36-8	DCD0	A2XA10P2-A7	P41-8	DCD0	A2XA11P2-A7	P46-8	DCD0	A2XA12P2-A7	P51-8	DCD0	
PORT 2	A2XA8P2-A12	P32-17	RXC1	A2XA9P2-A12	P37-17	RXC1	A2XA10P2-A12	P42-17	RXC1	A2XA11P2-A12	P47-17	RXC1	A2XA12P2-A12	P52-17	RXC1
	A2XA8P2-A9	P32-2	TXD1	A2XA9P2-A9	P37-2	TXD1	A2XA10P2-A9	P42-2	TXD1	A2XA11P2-A9	P47-2	TXD1	A2XA12P2-A9	P52-2	TXD1
	A2XA8P2-A14	P32-20	DTR1	A2XA9P2-A14	P37-20	DTR1	A2XA10P2-A14	P42-20	DTR1	A2XA11P2-A14	P47-20	DTR1	A2XA12P2-A14	P52-20	DTR1
	A2XA8P2-A16	P32-24	TXC1	A2XA9P2-A16	P37-24	TXC1	A2XA10P2-A16	P42-24	TXC1	A2XA11P2-A16	P47-24	TXC1	A2XA12P2-A16	P52-24	TXC1
	A2XA8P2-A10	P32-3	RXD1	A2XA9P2-A10	P37-3	RXD1	A2XA10P2-A10	P42-3	RXD1	A2XA11P2-A10	P47-3	RXD1	A2XA12P2-A10	P52-3	RXD1
	A2XA8P2-A11	P32-4	RTS	A2XA9P2-A11	P37-4	RTS	A2XA10P2-A11	P42-4	RTS	A2XA11P2-A11	P47-4	RTS	A2XA12P2-A11	P52-4	RTS
	A2XA8P2-A13	P32-5	CTS1	A2XA9P2-A13	P37-5	CTS1	A2XA10P2-A13	P42-5	CTS1	A2XA11P2-A13	P47-5	CTS1	A2XA12P2-A13	P52-5	CTS1
	A2XA8P2-C9	P32-7	GNDD1	A2XA9P2-C9	P37-7	GNDD1	A2XA10P2-C9	P42-7	GNDD1	A2XA11P2-C9	P47-7	GNDD1	A2XA12P2-C9	P52-7	GNDD1
A2XA8P2-A15	P32-8	DCD1	A2XA9P2-A15	P37-8	DCD1	A2XA10P2-A15	P42-8	DCD1	A2XA11P2-A15	P47-8	DCD1	A2XA12P2-A15	P52-8	DCD1	
PORT 3	A2XA8P2-A20	P33-17	RXC2	A2XA9P2-A20	P38-17	RXC2	A2XA10P2-A20	P43-17	RXC2	A2XA11P2-A20	P48-17	RXC2	A2XA12P2-A20	P53-17	RXC2
	A2XA8P2-A17	P33-2	TXD2	A2XA9P2-A17	P38-2	TXD2	A2XA10P2-A17	P43-2	TXD2	A2XA11P2-A17	P48-2	TXD2	A2XA12P2-A17	P53-2	TXD2
	A2XA8P2-A22	P33-20	DTR2	A2XA9P2-A22	P38-20	DTR2	A2XA10P2-A22	P43-20	DTR2	A2XA11P2-A22	P48-20	DTR2	A2XA12P2-A22	P53-20	DTR2
	A2XA8P2-A24	P33-24	TXC2	A2XA9P2-A24	P38-24	TXC2	A2XA10P2-A24	P43-24	TXC2	A2XA11P2-A24	P48-24	TXC2	A2XA12P2-A24	P53-24	TXC2
	A2XA8P2-A18	P33-3	RXD2	A2XA9P2-A18	P38-3	RXD2	A2XA10P2-A18	P43-3	RXD2	A2XA11P2-A18	P48-3	RXD2	A2XA12P2-A18	P53-3	RXD2
	A2XA8P2-A19	P33-4	RTS2	A2XA9P2-A19	P38-4	RTS2	A2XA10P2-A19	P43-4	RTS2	A2XA11P2-A19	P48-4	RTS2	A2XA12P2-A19	P53-4	RTS2
	A2XA8P2-A21	P33-5	CTS2	A2XA9P2-A21	P38-5	CTS2	A2XA10P2-A21	P43-5	CTS2	A2XA11P2-A21	P48-5	CTS2	A2XA12P2-A21	P53-5	CTS2
	A2XA8P2-C17	P33-7	GNDD2	A2XA9P2-C17	P38-7	GNDD2	A2XA10P2-C17	P43-7	GNDD2	A2XA11P2-C17	P48-7	GNDD2	A2XA12P2-C17	P53-7	GNDD2
A2XA8P2-A23	P33-8	DCD2	A2XA9P2-A23	P38-8	DCD2	A2XA10P2-A23	P43-8	DCD2	A2XA11P2-A23	P48-8	DCD2	A2XA12P2-A23	P53-8	DCD2	
PORT 4	A2XA8P2-A28	P34-17	RXC3	A2XA9P2-A28	P39-17	RXC3	A2XA10P2-A28	P44-17	RXC3	A2XA11P2-A28	P49-17	RXC3	A2XA12P2-A28	P54-17	RXC3
	A2XA8P2-A25	P34-2	TXD3	A2XA9P2-A25	P39-2	TXD3	A2XA10P2-A25	P44-2	TXD3	A2XA11P2-A25	P49-2	TXD3	A2XA12P2-A25	P54-2	TXD3
	A2XA8P2-A30	P34-20	DTR3	A2XA9P2-A30	P39-20	DTR3	A2XA10P2-A30	P44-20	DTR3	A2XA11P2-A30	P49-20	DTR3	A2XA12P2-A30	P54-20	DTR3
	A2XA8P2-A32	P34-24	TXC3	A2XA9P2-A32	P39-24	TXC3	A2XA10P2-A32	P44-24	TXC3	A2XA11P2-A32	P49-24	TXC3	A2XA12P2-A32	P54-24	TXC3
	A2XA8P2-A26	P34-3	RXD3	A2XA9P2-A26	P39-3	RXD3	A2XA10P2-A26	P44-3	RXD3	A2XA11P2-A26	P49-3	RXD3	A2XA12P2-A26	P54-3	RXD3
	A2XA8P2-A27	P34-4	RTS3	A2XA9P2-A27	P39-4	RTS3	A2XA10P2-A27	P44-4	RTS3	A2XA11P2-A27	P49-4	RTS3	A2XA12P2-A27	P54-4	RTS3
	A2XA8P2-A29	P34-5	CTS3	A2XA9P2-A29	P39-5	CTS3	A2XA10P2-A29	P44-5	CTS3	A2XA11P2-A29	P49-5	CTS3	A2XA12P2-A29	P54-5	CTS3
	A2XA8P2-C25	P34-7	GNDD3	A2XA9P2-C25	P39-7	GNDD3	A2XA10P2-C25	P44-7	GNDD3	A2XA11P2-C25	P49-7	GNDD3	A2XA12P2-C25	P54-7	GNDD3
A2XA8P2-A31	P34-8	DCD3	A2XA9P2-A31	P39-8	DCD3	A2XA10P2-A31	P44-8	DCD3	A2XA11P2-A31	P49-8	DCD3	A2XA12P2-A31	P54-8	DCD3	

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SIGNAL DEFINITION

- RXC - RECEIVING CLOCK
- TXD - TRANSMIT DATA
- DTR - DATA TRANSMISSION READY
- TXC - TRANSMITTING CLOCK
- RXD - RECEIVE DATA
- RTS - REQUEST TO SEND
- CTS - CLEAR TO SEND
- GND - GROUND
- DCD - DATA CARRIER DETECT

Figure 2.4.4. SIO Boards 4 Through 8 Ports and Pin Assignments (Sheet 2)

2.4.3.2.5 **Video Board.** The video board is an option that is installed on systems connected to airline video displays. The video board functions as the interface between the VMEbus and the airline video displays. The airline video displays are updated once per minute. The video display is memory mapped.

The video board consists of eight functional areas: data buffer, bus cycle control, address buffer and decode logic, memory, video timing and control, clock, RTC battery backup, and interrupt logic. The data buffer, bus cycle control, and address buffer and decode logic provide the standard address, data, and control signals necessary for system bus communication. The memory provides the storage for the display information. Each character location has a specific memory location. The data stored in memory are used to select a specific character and how it is displayed. The video timing and control provides the sync signals (horizontal and vertical) and display timing signals as well as memory address refresh. These discrete video signals are combined and output as a composite video signal. The clock and battery backup are not used.

The ACU CST checks the status of the video board once per minute. CST results are displayed on the video (graphics) page of the OID. The CST performs five tests: CRT CONTROLLER READBACK, PARALLEL I/F TIMER READBACK, LOOPBACK #1 and #2, and RT CLOCK READBACK. The technician can manually run the video memory test from the video page at any time. A T status is displayed for each test category until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The CRT CONTROLLER READBACK test reads the contents of a register in a CRT controller in the video timing and control area of the board. The status word is evaluated and the test status is displayed. The PARALLEL I/F TIMER READBACK test checks the operation of a parallel interface on the board. This parallel interface is not used. The LOOPBACK #1 and #2 tests check the status of two RS-422 SCC's provided by the board. These SCC's are not used by the system. The RT CLOCK READBACK tests clock timing. This clock is not used by the system.

2.4.3.2.6 **Digital I/O Board.** The digital I/O board provides address buffer and control, a data buffer, timing and interrupt control, two dual I/O port IC's (#1 and #2), and four transceivers. The CPU communicates with the digital I/O board over the VMEbus via the address buffer and decode, the data buffer, and the timing and interrupt control. The two dual I/O port IC's provide a total of four ports (ports A1, B1, A2, and B2), each of which communicates with external devices via a dedicated transceiver. Port A1 is configured as an input only port. This port is used by the CPU to input a watchdog timer signal from the voice processor board and to input status bits for the dc power supplies (via the VME resistor board) and the UPS bypass circuit. Port B1 is configured as an output only port. This port is used by the CPU to output control signals to the voice recorder/playback board, the rf modem switch (or line driver relay), and the UPS bypass circuit. Ports A2 and B2 on the DIO board are not used in the ACU. The ACU CST does not check the status of the digital I/O board. §
§

2.4.3.2.7 **A/D Board and VME Resistor Board.** The A/D board and the VME resistor board make up the ACU power and signal monitoring function. The A/D board, in conjunction with the VME resistor board, receives dc power monitor signals and converts them to digital values that may be read by the CPU via the VMEbus. A detailed description of these boards is provided in the ACU power and signal monitoring description (paragraph 2.4.3.8).

2.4.3.3 **Digital Voice Processor System.** The digital voice processor (Figure 2.4.5) is made up of Voice Processor Board A20 and Voice Recorder/Playback Board A21. These two boards operate together as a system and are tested together. They are both connected to the VMEbus for power and system reset purposes, but they do not communicate with the CPU via the VMEbus. CPU/voice system communication is accomplished via the RS-232 link between SIO board 2 and the voice processor board.

2.4.3.3.1 Voice Processor Board. The voice processor board contains a Z80XXX series (Z80 thousand series) microprocessor and the necessary memory to execute onboard instructions. These instructions are used to reconstruct digitized human voice, create voice reports, and receive operator-generated digitized audio from the voice recorder/playback board. The voice processor board communicates with the VMEbus directly for power and system reset and indirectly via SIO board 2 for system communication. The following paragraph provides a detailed block diagram description of the voice processor board.

The voice processor board consists of nine functional areas (Figure 2.4.5): system reset/power interface, DRAM, EPROM vocabulary, CPU, audio board interface, timing and control logic, serial communications controller, RS-232 driver and receiver logic, and watchdog timer and alarm. The system reset/power interface generates an internal reset when the system reset signal from the VMEbus is received or the RESET pushbutton switch on the front of the board is pressed and power is applied. The internal reset disables message broadcast until a play message string is received from the CPU via SIO board 2. The VMEbus interface for power and ground requirements is also provided by the system reset/power interface. The DRAM provides 1 Mbyte of memory for message/file storage. This is the area where digitized messages from the FAA handset are stored. These messages are appended to the automatically generated observation messages. The EPROM vocabulary consists of 512 Kbytes of EPROM for voice files. The onboard CPU executes the operational software to execute new message strings and to monitor the eight telephone lines. The audio board interface provides the communication path to the voice recorder/playback board via the 50-pin connector on the front of the board. The necessary timing and interface signals required by the CPU and peripherals are provided by the timing and control logic. The serial communications controller provides the RS-232 serial communication channel, and the RS-232 driver and receiver logic provides the standard RS-232 receive and transmit lines. The watchdog timer and alarm provides an alarm signal to the primary CPU (via Digital I/O Board 1A2A15) when a CPU software or hardware failure occurs.

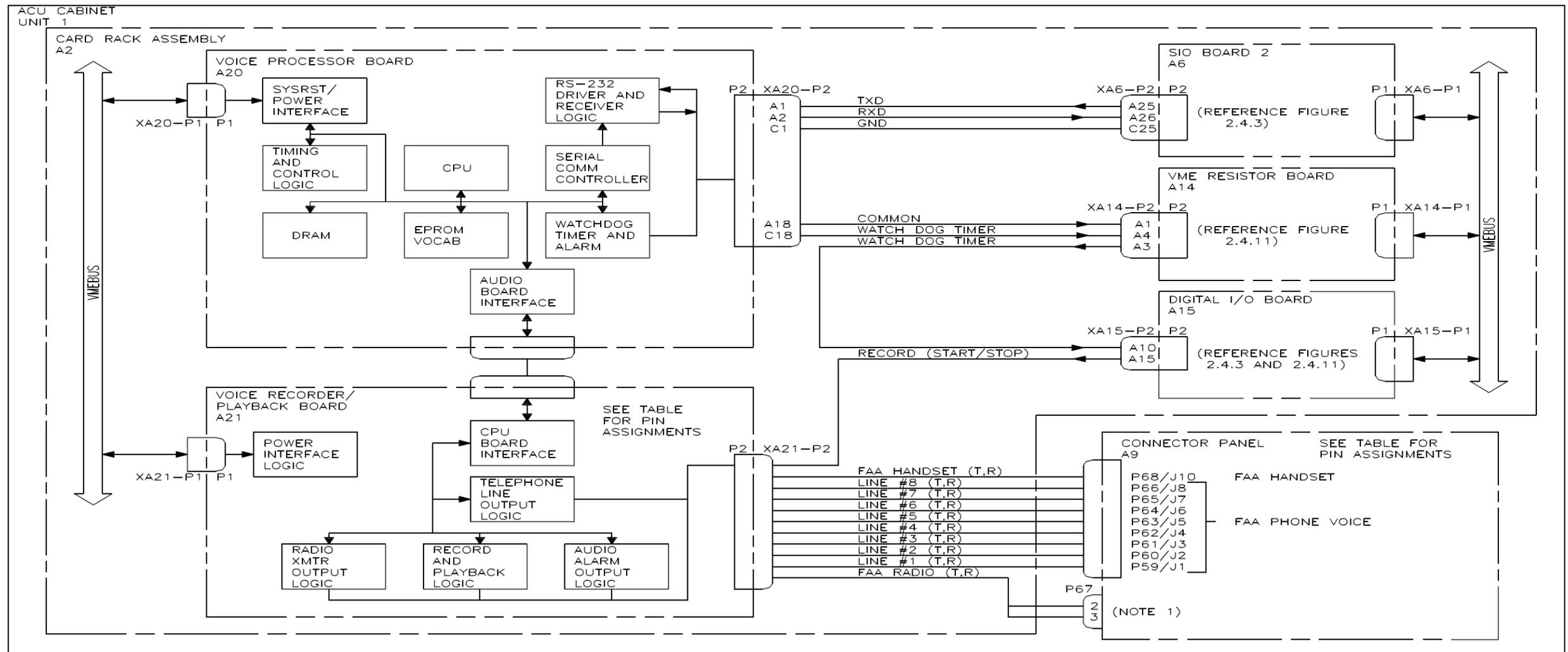
2.4.3.3.2 Voice Recorder/Playback Board. The voice recorder/playback board receives digitized voice from the voice processor board and converts it into audio. Audio is output as a weather data message for dial-in weather requests and to a VHF transmitter for airline use. In addition, the voice recorder/playback board receives audio signals from the FAA handset and transmits the digitized audio to the voice processor board for processing. The following paragraph provides a detailed block diagram description of the voice recorder/playback board.

The voice recorder/playback board consists of six functional areas (Figure 2.4.5): CPU board interface, power interface logic, radio transmitter output logic, record and playback logic, telephone line output logic, and audio alarm output logic. Pinouts for the output of the voice recorder/processor board (XA21-P2) are provided on the table on figure 2.4.5. The signal mnemonics and pins associated with row A and row C of XA21-P2 are listed with the associated plug connector. For example, the RING signal of the FAA handset line can be monitored at pin 20 of XA21-P2 or pin 2 of plug 68 (P68). The CPU board interface provides the communication path to the voice processor board via the 50-pin connector on the front of the board. The VMEbus interface for power and ground requirements is provided by the power interface logic. The radio transmitter output logic and the record and playback logic digitize audio input and synthesize digitized voice to audio. The interface circuits to the telephone outputs and line output peripherals are provided by the telephone line output logic. The audio alarm output logic provides an audio alarm indicator. One of the audio line outputs is continually monitored by the alarm circuit. A loss of audio for a predetermined period causes the indicator on the voice recorder/playback board to illuminate. Chapter 12 provides information on GTA radio pin-to-pin connections.

XA21-P2 TO P59-68 PIN ASSIGNMENTS

XA21-P2 PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW A P1 THROUGH P10 PIN NUMBERS	ROW C SIGNAL MNEMONIC	ROW C P1 THROUGH P10 PIN NUMBERS
20	RING, FAA HANDSET	P68-2	FAA HANDSET	P68-3
24	RING, FAA RADIO	P67-2	FAA RADIO	P67-3
25	RING, LINE #8	P66-2	LINE #8	P66-3
26	RING, LINE #7	P65-2	LINE #7	P65-3
27	RING, LINE #6	P64-2	LINE #6	P64-3
28	RING, LINE #5	P63-2	LINE #5	P63-3
29	RING, LINE #4	P62-2	LINE #4	P62-3
30	RING, LINE #3	P61-2	LINE #3	P61-3
31	RING, LINE #2	P60-2	LINE #2	P60-3
32	RING, LINE #1	P59-2	LINE #1	P59-3

NOTE:
1. REFER TO CHAPTER 12, FIGURE 12.4.2, FOR CONNECTION POINTS.



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Figure 2.4.5. Digital Voice Processor Detailed Block Diagram

2.4.3.3.3 Testing the Digital Voice Processing System. The ACU CST checks the status of the digital voice processing system once per minute. CST results are displayed on the voice page of the OID. The CST performs four tests on the voice processing system: CPU, AUDIO OUTPUT, AUDIO STATUS, and TIMEOUT. The technician can manually run the voice processing test from the VOICE page at any time. A T status is displayed for the four test categories until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The CPU test checks the operational status of the voice processor board. The TIMEOUT test checks the operational status of the watchdog timer. The AUDIO OUTPUT and AUDIO STATUS tests check the operation of the voice recorder/playback board and indirectly test the voice processor board. The AUDIO OUTPUT test is based on an internal audio test that checks the audio circuitry. The AUDIO STATUS test is based upon a monitored audio line. The status of each test is evaluated and the test status is displayed.

2.4.3.4 Modem Communications. Three different types of modem communications are provided in the ACU cabinet: modems for telephone communications, rf communications, and dedicated line communications. The system is configured with rf modems or line drivers (commonly referred to as short haul modems); it does not contain both. The following paragraphs provide a detailed block diagram description of the modems and their modes of operation.

2.4.3.4.1 Telephone Modems. Modem AC Power Rack 1A3 can contain up to 10 telephone modems (Figure 2.4.6) which operate in a 2-wire full duplex mode over both leased lines and the public switched network. The modems provide communications to external devices over leased line or public switched telephone network at data rates of 2400, 9600, or 28800 baud (models 2440, V.3225, and V.3400 respectively). All data transfers are under the control of the SIO boards, which communicate with the data terminal equipment (DTE) ports of the modems using RS-232 protocol.

In most cases, the modems used are model 2440 devices, which operate at data rates of up to 2400 baud. Modems 1A3A4 and A5 are provided in all systems, and are dedicated as USER PHONE #1 (model 2440) and #2 (model 2440 or V.3400). These modems are controlled by port 3 of SIO boards 2 (A6) and 3 (A7). The outputs of these modems are connected to J15 and J16 of I/O Panel Assembly 1A9. Sheet 1 of figure 2.4.6 illustrates the installation of the model 2440 and V.3400 modems.

All of the other modems are optional and are installed in the system as required to provide the following ports:

- a. AFOS phone
- b. OID spare
- c. ADAS
- d. VDU's
- e. AWIPS
- f. User Phone #1 spare
- g. User Phone #2 spare
- h. Printer

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These modems are controlled by SIO boards 4 through 8. Their outputs are connected to connectors J12 through J14 and J17 through J21 of I/O Panel Assembly 1A9.

As stated above, model 2440 modems are used for most ASOS telephone communication applications. The

exceptions are USER PHONE #2 at selected sites which uses the 28800 baud modem (model V.3400) and optional secondary OID's (OID #2, port 3B, and OID #3, port 3C) which use the 9600 baud modem (V.3225). When secondary OID ports are active, model V.3225 modems are installed in modem rack slots A2 and A3. Leased line connections are made at connectors J13 and J14 of I/O Connector Panel 1A9. Sheet 2 of figure 2.4.6 illustrates the configuration of an ACU that has been modified to accept V.3225 modems (9600 baud) in slots A2 and A3. This modification is performed for ACU's (Class I and Class II) having serial numbers 364 and below. Sheet 3 of figure 2.4.6 shows the configuration of an ACU for which the V.3225 modems were built in as original equipment. This configuration applies to Class I and Class II ACU's with serial numbers 365 and above.

The ACU CST checks the status of the telephone modems configured for dial-up operation (leased line modems are always on-line and cannot be tested). CST results for the dial-up modems are displayed on the MODEM RACK page of the OID. Each modem is tested once every 7 minutes, as long as the modem is not busy (no user is logged onto the system). If the modem is busy during a CST cycle, the CST is not performed. This is because running the CST on an active modem disrupts the communications and valuable information may be lost.

The test that is performed during CST is an analog self-test loopback test. The CPU initiates the test, but the entire test is performed inside the modem. The transmitter in the modem is internally linked to the receiver. The modem then generates a test pattern, transmits it over the loopback, receives the data, and checks for errors. The modem completes the test by reporting its pass/fail status back to the CPU. The CPU then displays the status on the MODEM RACK page. A status of D (degraded) is displayed for a modem if five or more failures have been detected and the modem is currently passing its loopback test. At 0600 LST each day, the number of accumulated failures is summarized in the system (maintenance) log. Chapter 1, Section III provides additional information on SIO test reporting.

In addition to the regular CST testing, the technician may manually initiate a test of a dial-up modem from the MODEM RACK page. When a test is ordered, the modem immediately tests itself as described above. As mentioned before, if the modem is busy when the test is ordered, current communications are disrupted as the test is performed. For this reason, the technician should ensure that the modem is not in use before manually issuing a test command. The LCD indicator on the front of the modem which should indicate OFF-LINE can be used to verify that the modem is not in use.

§ 2.4.3.4.2 **RF Modems.** Three different rf modems are used in two ACU configurations. The modems are § 62828-90013-XX (AAI Corporation), 62828-90315-XX (Motorola, Inc), or 62828-40506-X (Johnson Data). § ACU -10 cabinets (62828-40044-10) serial number 185 and below and ACU -20 cabinets (62828-40044-20) § serial number 245 and below were originally manufactured with AAIrf modems. The -10 cabinets with serial § numbers 186 and above and the -20 cabinets with serial numbers 246 and above were manufactured with § Motorola modems.

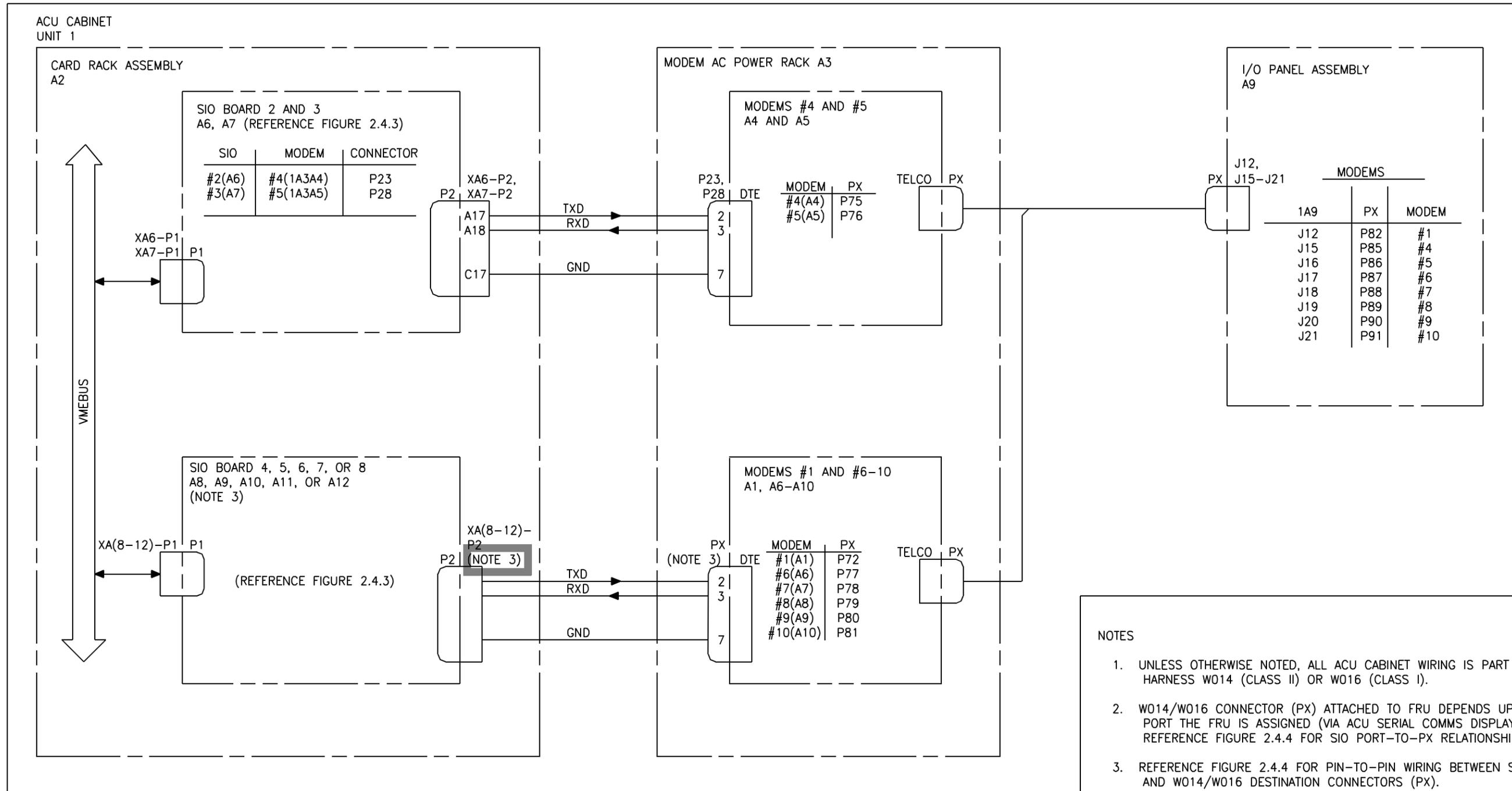
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§ Normally, a system built with AAI modems continues to operate with the modems until sufficient spares can § no longer be obtained. When this occurs, the entire site (ACU and DCP) must be modified to operate with § Motorola modems. This modification is accomplished by the installation of FMK 18886. This FMK § an be ordered through NLSC using ASN S100-FMK18886. Each kit contains adapter cables W050 (to route § signals and power from the existing harness to the new modems) and two modems (the quantity required to § complete a Class I system). Two FMK's must be ordered to upgrade a Class II system. All AAI modems § removed from a system must be returned to the National Reconditioning Center.

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MODEL 2440 MODEM INSTALLATION



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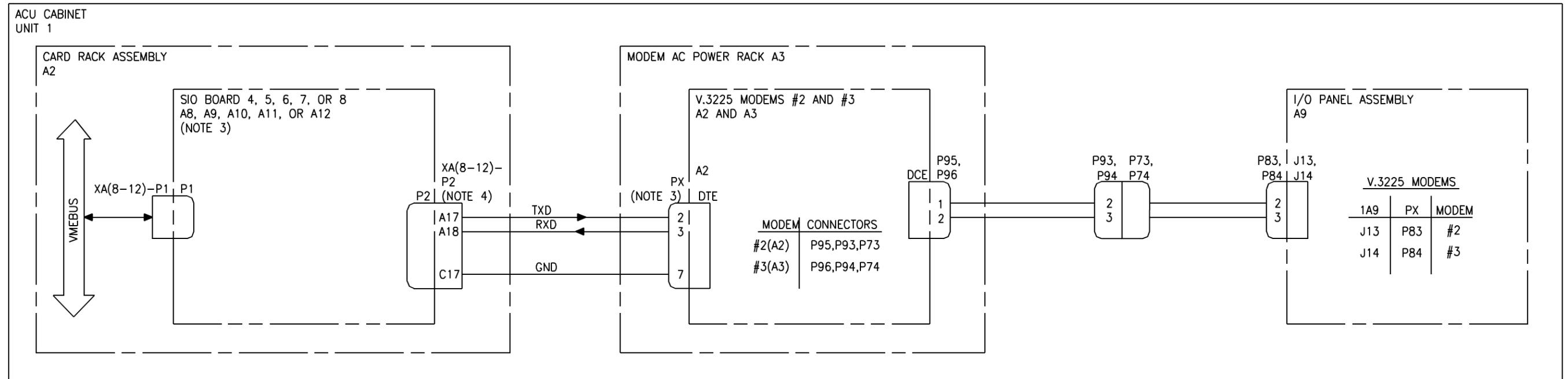
Figure 2.4.6. Leased Line and Public Switched Telephone Modem Communications Detailed Block Diagram (Sheet 1 of 3)

V.3225 MODEM INSTALLATION

NOTE

1. SHEET 2

9600 BAUD RETROFIT INSTALLED ON S/N 364 AND BELOW



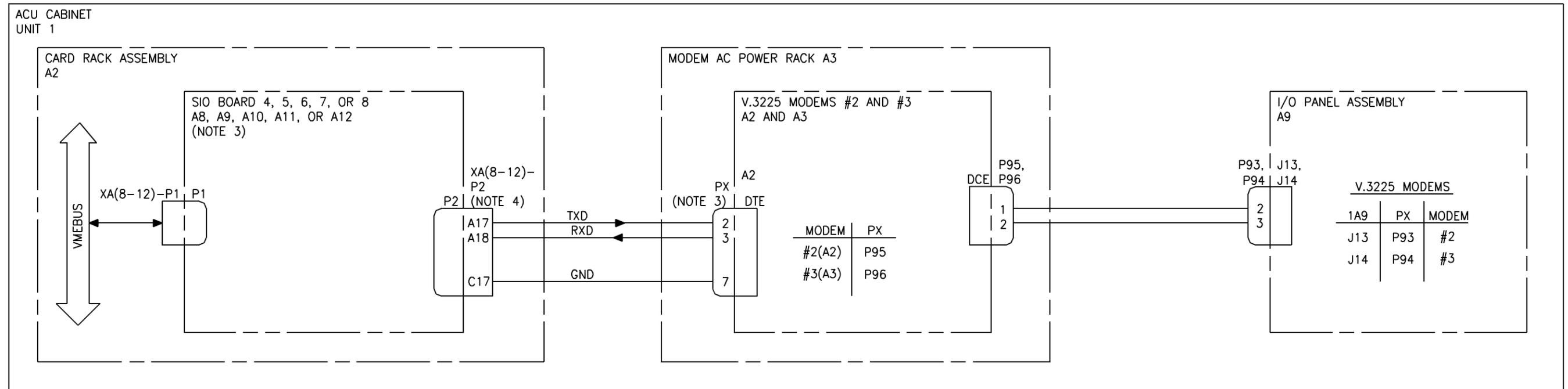
5202F06

Figure 2.4.6. Leased Line and Public Switched Telephone Modem Communications Detailed Block Diagram (Sheet 2)

V.3225 MODEM INSTALLATION

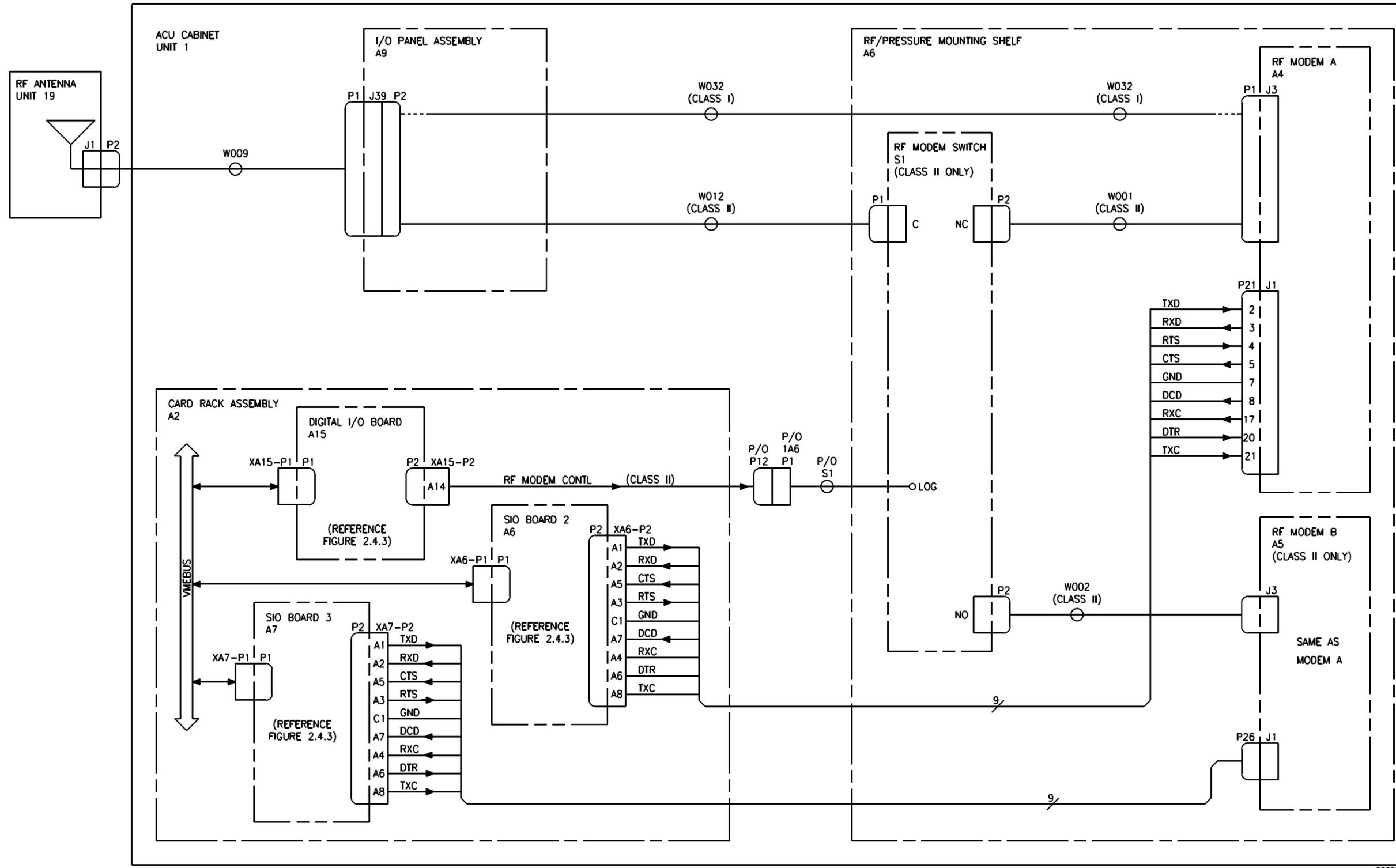
NOTE

- 1. SHEET 3
- S/N 365 AND ABOVE



5202F07

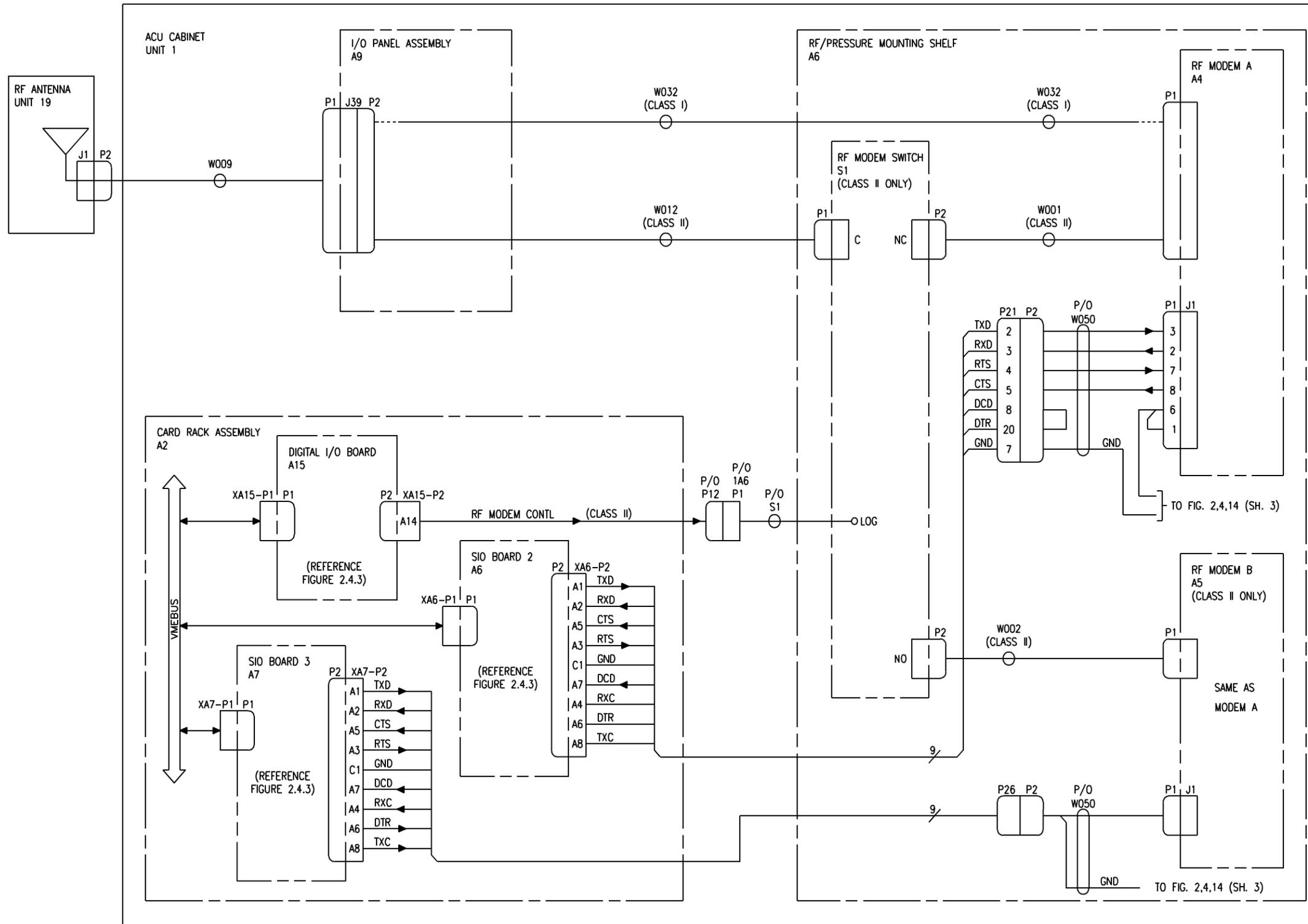
Figure 2.4.6. Leased Line and Public Switched Telephone Modem Communications Detailed Block Diagram (Sheet 3)



- NOTES
- UNLESS OTHERWISE NOTED, ALL ACU CABINET WIRING IS PART OF HARNESS W014 (CLASS II) OR W016 (CLASS I).
 - SIGNAL DESCRIPTION
 TXD - TRANSMIT DATA
 RXD - RECEIVE DATA
 CTS - CLEAR TO SEND
 RTS - REQUEST TO SEND
 GND - GROUND
 DCD - DATA CARRIER DETECT
 RXC - RECEIVING CLOCK
 DTR - DATA TERMINAL READY
 TXC - TRANSMIT CLOCK
 - SHEET 1
 ACU 62828-40044-10:
 S/N 185 AND BELOW
 ACU 62828-40044-20:
 S/N 245 AND BELOW
 - TO REDUCE COCHANNEL INTERFERENCE, OPTIONAL FIVE WATT ATTENUATORS MAY BE INSERTED IN THE ANTENNA LINE(S) TO REDUCE TRANSMIT POWER INTO THE ANTENNAS.

AAI MODEMS

Figure 2.47. ACU RF Modem/Line Driver Communications Link Detailed Block Diagram (Sheet 1 of 6)

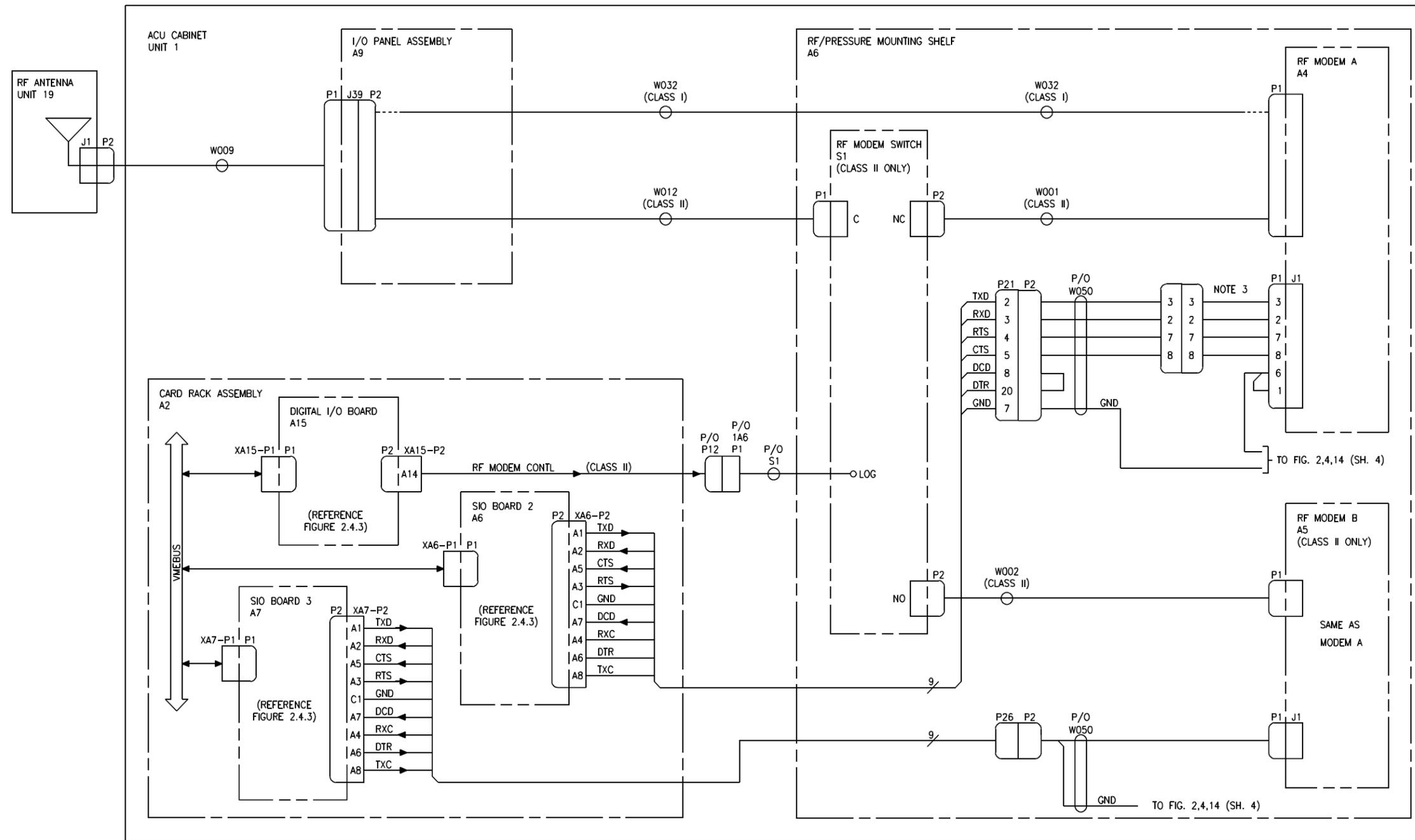


- NOTE
1. SHEET 2
 FMK 18886 INSTALLED ON
 ACU 62828-40044-10:
 S/N 185 AND BELOW
 ACU 62828-40044-20:
 S/N 245 AND BELOW
 2. TO REDUCE COCHANNEL INTERFERENCE, OPTIONAL FIVE WATT ATTENUATORS MAY BE INSERTED IN THE ANTENNA LINE(S) TO REDUCE TRANSMIT POWER INTO THE ANTENNAS

5202E02

**SYSTEM CONVERTED FROM AAI
 MOTOROLA MODEMS**

**Figure 2.4.7. ACU RF Modem/Line Driver
 Communications Link Detailed Block
 Diagram (Sheet 2 of 6)**



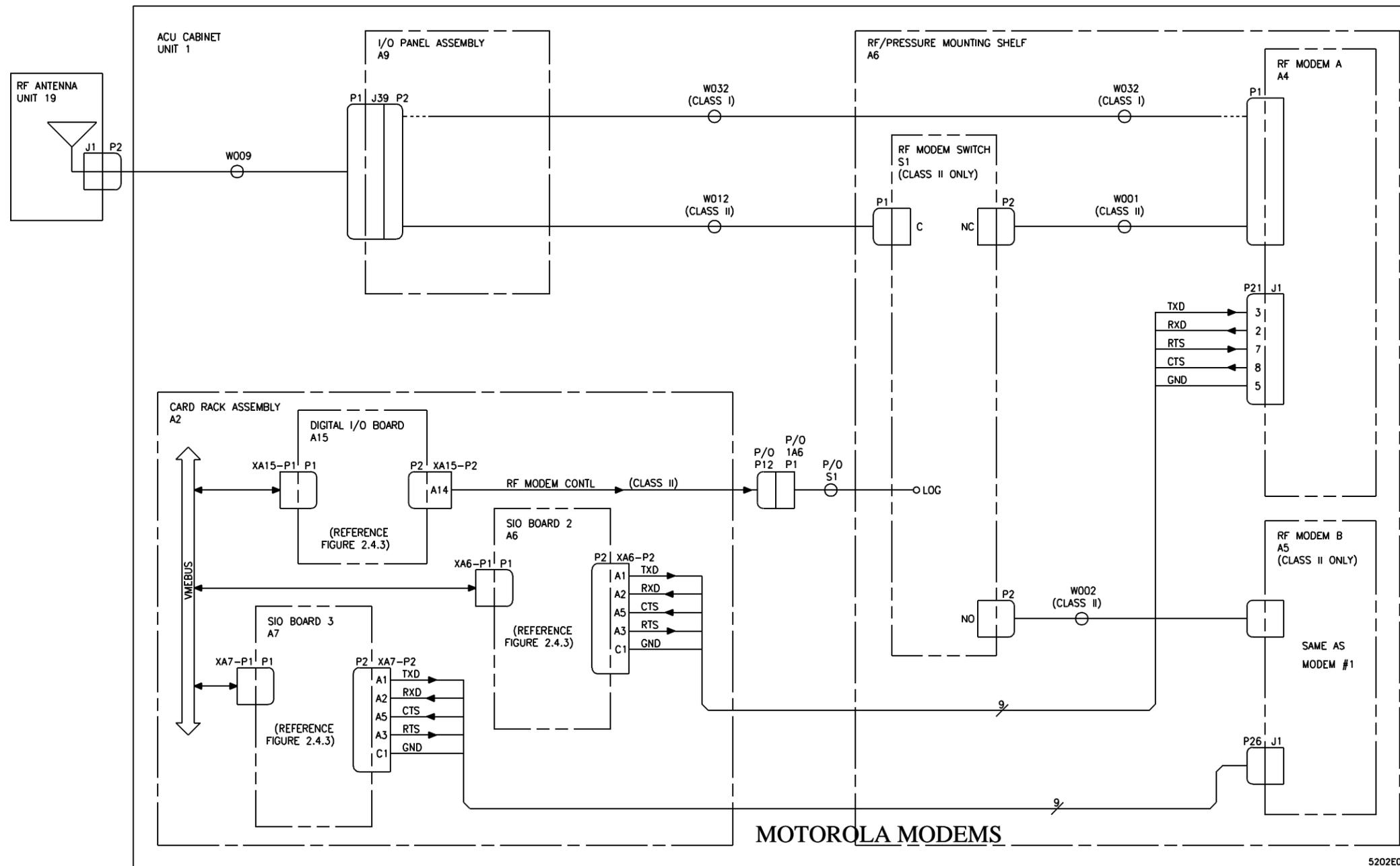
NOTE

1. FMK 18886 INSTALLED ON ACU 62828-40044-10: S/N 185 AND ABOVE
ACU 62828-40044-20: S/N 245 AND ABOVE
2. TO REDUCE COCHANNEL INTERFERENCE, OPTIONAL FIVE WATT ATTENUATORS MAY BE INSERTED IN THE ANTENNA LINE(S) TO REDUCE TRANSMIT POWER INTO THE ANTENNAS
3. ADAPTER CABLE 62828-42110-10 INSTALLED BETWEEN W50P1 AND RF MODEM.

5202E02-1

SYSTEM CONVERTED FROM AAI TO MOTOROLA MODEMS EQUIPED WITH JOHNSON DATA MODEMS

Figure 2.4.7. ACU RF Modem/Line Driver Communications Link Detailed Block Diagram (Sheet 3 of 6)

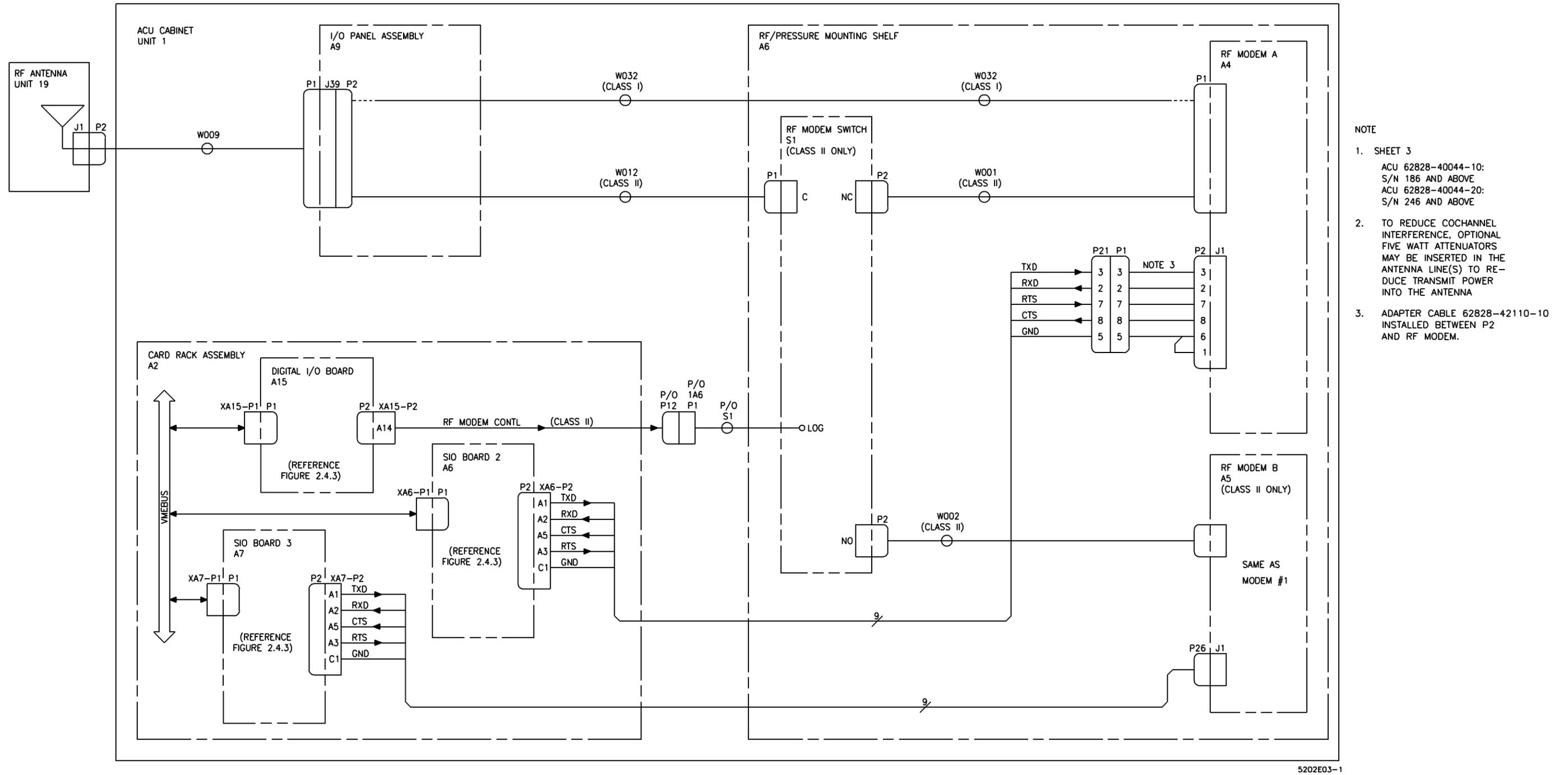


NOTE

1. SHEET 3
 ACU 62828-40044-10:
 S/N 186 AND BELOW
 ACU 62828-40044-20:
 S/N 246 AND BELOW
2. TO REDUCE COCHANNEL INTERFERENCE, OPTIONAL FIVE WATT ATTENUATORS MAY BE INSERTED IN THE ANTENNA LINE(S) TO REDUCE TRANSMIT POWER INTO THE ANTENNA

5202E03

Figure 2.4.7. ACU RF Modem/Line Driver Communications Link Detailed Block Diagram. (Sheet 4 of 6)

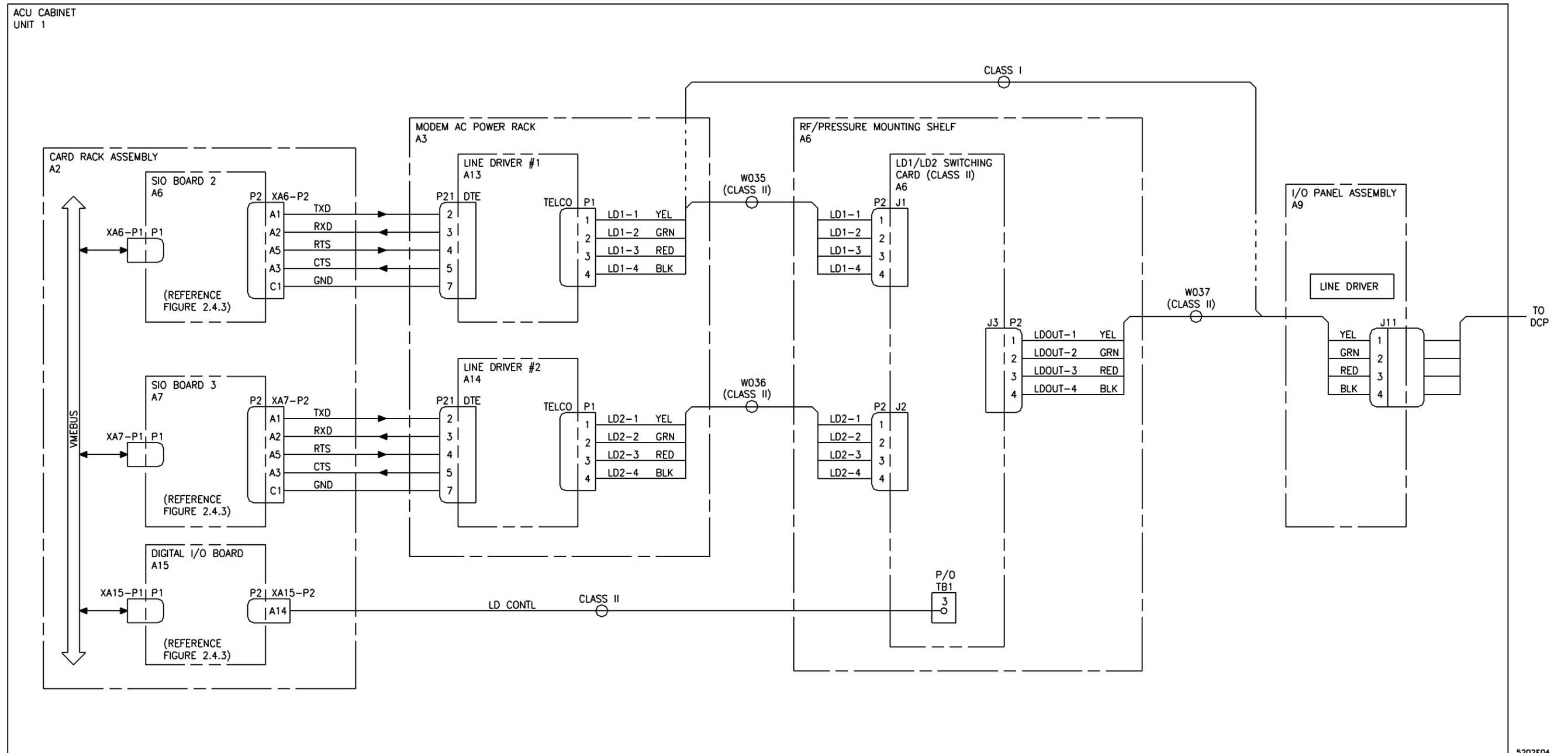


- NOTE
1. SHEET 3
ACU 62828-40044-10:
S/N 186 AND ABOVE
ACU 62828-40044-20:
S/N 246 AND ABOVE
 2. TO REDUCE COCHANNEL INTERFERENCE, OPTIONAL FIVE WATT ATTENUATORS MAY BE INSERTED IN THE ANTENNA LINE(S) TO REDUCE TRANSMIT POWER INTO THE ANTENNA
 3. ADAPTER CABLE 62828-42110-10 INSTALLED BETWEEN P2 AND RF MODEM.

5202E03-1

**CONVERTED FROM MOTOROLA MODEMS
TO JOHNSON DATA MODEMS**

**Figure 2.4.7. ACU RF Modem/Line Driver
Communications Link Detailed Block Diagram
(Sheet 5 of 6)**



5202E04

Figure 2.4.7. ACU RF Modem/Line Driver Communications Link Detailed Block Diagram (Sheet 6 of 6)

For a Class II system, the ACU rf communications equipment consists of two rf modems (A and B), an rf modem switch, and an omnidirectional antenna (Figure 2.4.7, sheets 1 through 6. Omnidirectional antennas are usually used in the ACU-DCP rf link. However, at certain sites where RFI was experienced, yagi antennas are used at one or both ends of the link. A yagi can only be used at the ACU if all DCP's are illuminated within the yagi's 10-degree beamwidth. A seven-element yagi, PN 62828-90413-2, provides 10 dB gain over the 406 - 420 MHz band and has a front:back ratio of 14 dB. Additionally, at sites where cochannel interference is particularly troublesome, five watt attenuators of 3 dB, 6 dB, 10 dB, 20 dB, or 30 dB (PN 62828-90424 -2, -3, -4, -5, and -6, respectively) may be inserted in the antenna line(s) to reduce transmit power into the antennas. The rf modems are identical, with one modem serving as the primary communications link and the other as a backup. The test is based on a loop test. The ACU transmits a predefined pattern across the communications link, and the DCP verifies modems operate in the UHF frequency range in half duplex mode. The primary CPU communicates with rf modem A via SIO board 2 and with modem B via SIO board 3. The rf switch selects which modem uses the antenna. The switch is controlled by the CPU via DIO board A15. In the event that the primary CPU senses a failure in its primary rf link (no data received for a period of 2-1/2 minutes), it writes a selection word to the DIO board to toggle the rf switch. The other modem then becomes the primary modem and controls all rf communications between the DCP and ACU. For a Class I system, the rf communications circuitry is similar, except there is no redundant rf system (there is only one rf modem and no rf switch).

§

The ACU CST checks the status of the ACU/DCP communications link once per minute. CST results are displayed on the ACU/DCP COMM page of the OID. This test performs two checks: RADIO A OR L/D A and RADIO B OR L/D B. The RADIO A OR L/D A test checks the A link between the ACU and up to three DCP's. The RADIO B OR L/D B test does the same for link B (Class II systems only). The CST also identifies which link (modem or line driver) (A or B) is currently serving as the primary link in the ACU and all DCP's.

The rf communications the reception of the pattern by responding with an OK or ERROR acknowledgment. An incorrect reception signifies an error and a failed indication. A failed indication is also displayed if the DCP fails to respond at all to the ACU transmission.

2.4.3.4.3 Line Drivers. If dictated by the configuration, two line drivers and an LD1/LD2 switching board (Figure 2.4.7, sheet 6) are used in place of rf modems and the rf modem switch. The line drivers in the ACU are connected by a direct line to corresponding line drivers in the DCP. The line drivers are commonly referred to as short haul modems and perform a function similar to that of the rf modems. Diagnostically, the line driver is tested in lieu of the rf modem and the status is displayed on the ACU/DCP COMM page. The diagnostic test is the same as that used for the rf modems.

§

Normally, a system built with UDS D19.2 line drivers continues to operate with the line drivers until sufficient spares can no longer be obtained. When this occurs, the entire site (ACU and DCP) must be modified to operate with Motorola DDS/MR64 line drivers as detailed in Field Modification Kit FMK 086. This FMK can be ordered through NLSC. Each kit contains two line drivers required to update a Class I system. Order two kits to upgrade a Class II system. All UDS line drivers removed from a system must be returned to the National Reconditioning Center.

2.4.3.5 Pressure Sensors. The rf/pressure mounting shelf is a slide-mounted rack containing up to three barometric pressure sensors (Figure 2.4.8). Three pressure sensors are installed in Class II systems, while Class I systems have pressure sensors 1 and 2 only. The pressure sensors provide barometric pressure in inches of mercury (inHg). The primary CPU communicates with pressure sensors 1 and 2 via RS-232 ports of SIO boards 2 and 3. Pressure sensor 3, when installed, communicates with the CPU via one of the optional SIO boards (4 through 8). An adapter cable (W026) is used for pressure sensor 3 data. This cable adapts the 25-pin RS-232 connector for the optional SIO port to the 9-pin RS-232 connector on the pressure sensor. The pressure connection is provided at the connector panel and is labeled PRESSURE PORT.

Pressure sensors that are installed in Class I ACU cabinets (without optional UPS) must be equipped with threshold detectors, which may be either internal (built into the sensor) or external. A threshold detector ensures that the pressure sensor resets completely in the event of a dc power undervoltage fluctuation (when

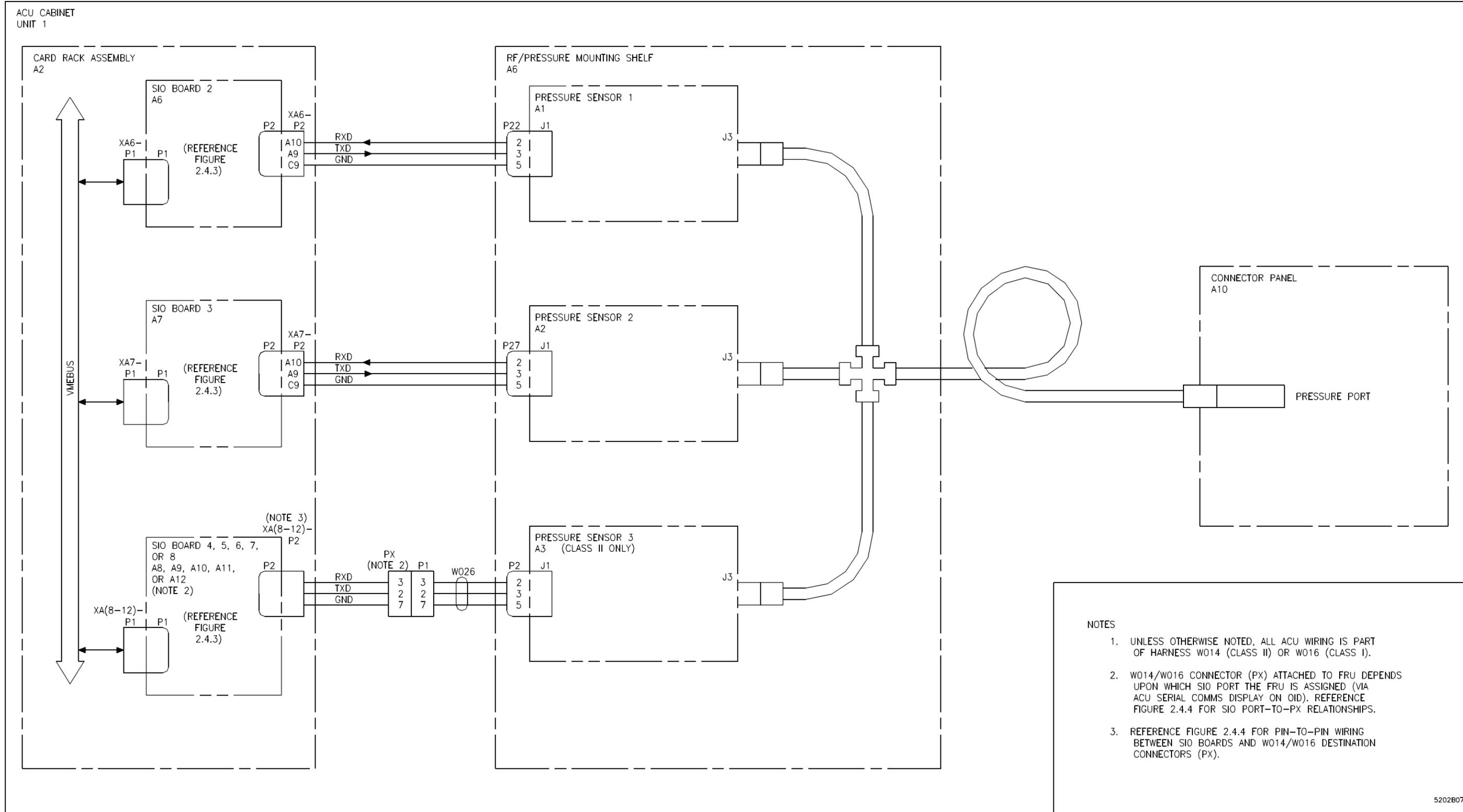
its power drops below 4.55 vdc). Threshold detectors are not required on Class II systems because the ACU's uninterruptible power supply prevents such fluctuations. Internal threshold detectors were built into pressure sensors with serial numbers 358495, 358509, and 363914 and above. Internal detectors are being added to all other sensors when they are returned to the depot for repair. In these cases, a label is applied to the repaired sensor, indicating that an internal detector has been added. External threshold detectors are installed on Class I systems via FMK #027. The external detector is a small module that is mounted to the sensor's DB-9 power connector (J2). The external detector then becomes part of the pressure sensor and should not be removed (it is not an FRU). As part of the FMK, a label is placed on the pressure sensor stating "EXTERNAL THRESHOLD DETECTOR REQUIRED". FMK 27 can be ordered through NLSC. Order S100-FMK27 for threshold detector and labels. Special authorization is required when ordering this kit.

The ACU CST displays the current status of the pressure sensors on the OID PRESSURE #1, #2, and #3 pages. Status is provided for three parameters: DATA QUALITY, REPORT PROCESSING, and SENSOR RESPONSE. The DATA QUALITY field displays the current status (pass/fail) of data quality checks performed by pressure sensor algorithm software. The REPORT PROCESSING field indicates Y if report processing is currently turned on (system reports sensor data) or indicates N if report processing has been manually turned off (system reports manually entered pressure data or "missing" if no manual data). The SENSOR RESPONSE field indicates an F if the CPU does not receive pressure sensor data responses.

2.4.3.6 Local Sensor Fiberoptic Modems. The local sensor fiberoptic modems provide fiberoptic ports for three additional local sensors (Figure 2.4.9). These fiberoptic modems are connected to RS-232 ports on the optional SIO boards (4 through 8). Adapter cables (W011) are used to adapt the 25-pin RS-232 connectors for the SIO ports to the 9-pin RS-232 connectors on the fiberoptic modems. Electrical data transmitted from an SIO board are converted to optical data and are then transferred to the connected device. Optical data received from the connected device are converted to electrical data and transmitted to the SIO board as received data.

2.4.3.7 Observer Notification Device and Peripheral Power. Figure 2.4.10 illustrates detailed wiring for the observer notification device (OND) and peripheral power strip W006. The OND is controlled by the CPU via a digital output signal from DIO Board A15. When the OND is to flash, the CPU repeatedly toggles this signal on and off. The printer, primary OID, and FAA modems (not part of the ASOS) may receive their power from power strip W006, which is connected to PERIPHERAL POWER connector J40 on I/O Panel Assembly 1A9. In Class II systems, connector J40 receives power from the UPS in Power Supply Assembly 1A4. As such, backup power is supplied to these peripherals in the event of a loss of primary ac power. The OND operates on 12 vdc, and therefore has a 12 vdc converter built into its power cord that plugs directly into any available ac wall outlet.

2.4.3.8 ACU Power and Signal Monitoring. The circuitry shown on the ACU power and signal monitoring detailed block diagram (Figure 2.4.11) interfaces with both analog voltage signals and digital data points to allow monitoring by system software. The hardware is used by the diagnostic software to read the status of dc power supply output voltages, the power applied to the rf modems, as well as UPS bypass circuit in Class II systems. Sheets 1 through 3 of figure 2.4.11 show three different configurations of power monitoring circuitry, depending on the rf modem installation (paragraph 2.4.3.4.2). Sheet 1 shows the configuration for original equipment AAI rf modems, sheet 2 illustrates a system that has been modified for Motorola modems, and sheet 3 shows the configuration for original equipment Motorola modems. The following paragraphs describe the operation of the ACU power and signal monitoring circuitry.

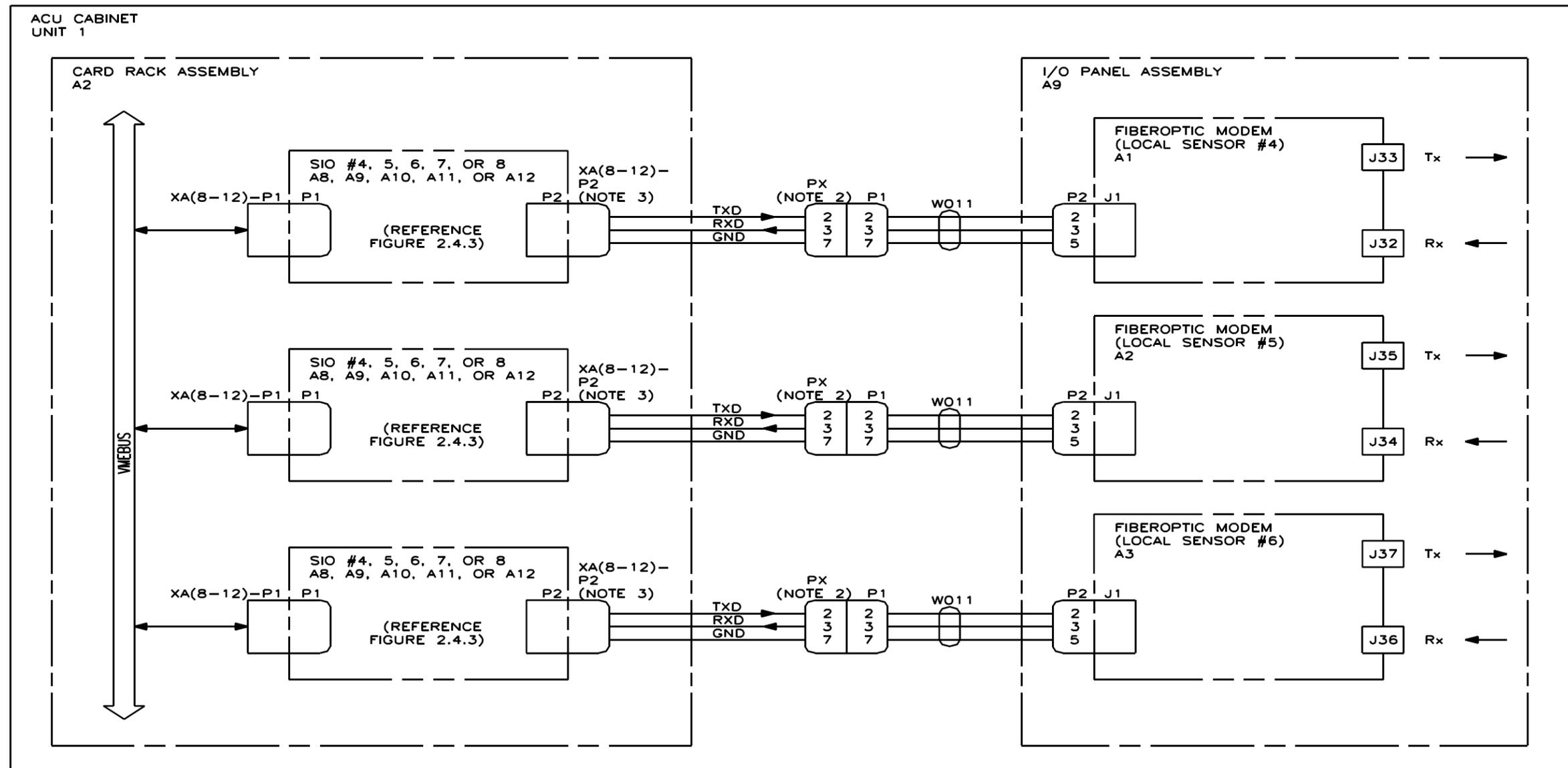


5202B07

Figure 2.4.8. Pressure Sensor Detailed Block Diagram

NOTES

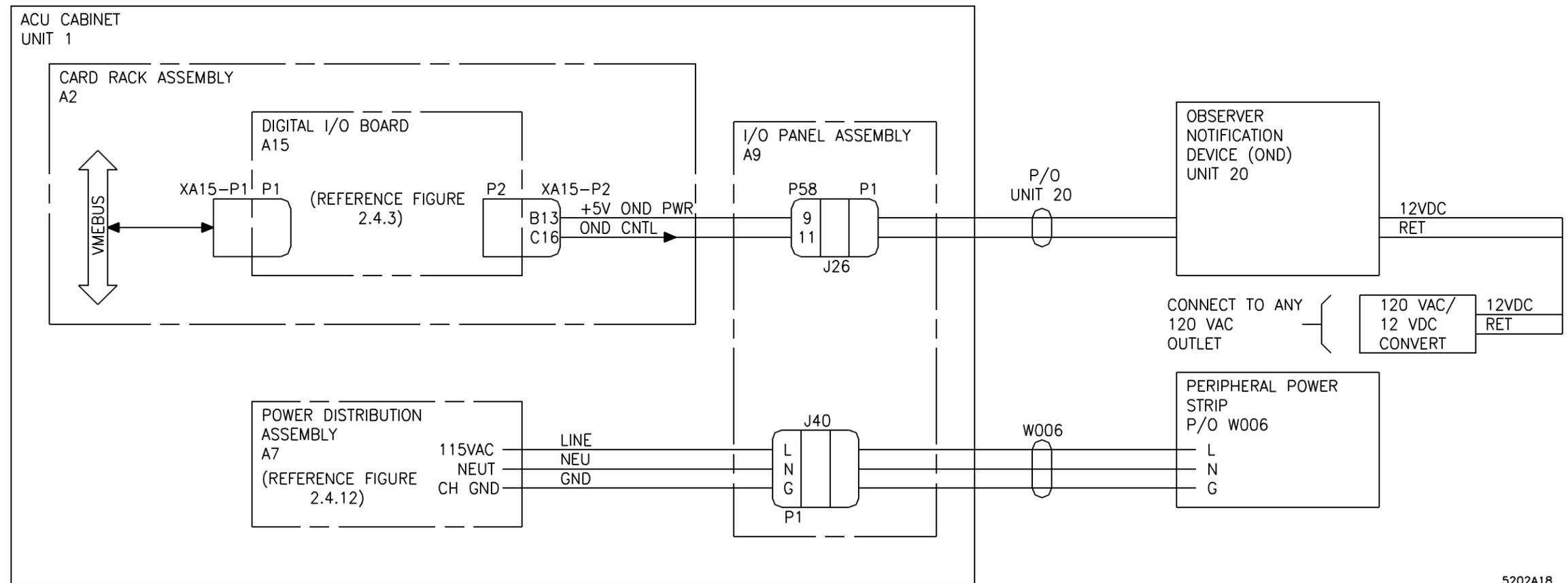
1. UNLESS OTHERWISE NOTED, ALL ACU WIRING IS PART OF HARNESS WO14 (CLASS II) OR WO16 (CLASS I).
2. WO14/WO16 CONNECTOR (PX) ATTACHED TO FRU DEPENDS UPON WHICH SIO PORT THE FRU IS ASSIGNED (VIA ACU SERIAL COMMS DISPLAY ON OID). REFERENCE FIGURE 2.4.4 FOR SIO PORT-TO-PX RELATIONSHIP.
3. REFERENCE FIGURE 2.4.4 FOR PIN-TO-PIN WIRING BETWEEN SIO BOARDS WO14/WO16 DESTINATION CONNECTORS (PX).
4. SIGNAL DESCRIPTION
 TXD - TRANSMIT DATA
 RXD - RECEIVE DATA
 GND - GROUND



5202A15

Figure 2.4.9. Local Sensor Fiberoptic Modem Detailed Block Diagram

1. UNLESS OTHERWISE NOTED, ALL ACU CABINET WIRING IS PART OF HARNESS W014 (CLASS II) OR W016 (CLASS I).
2. W014/W016 CONNECTOR (PX) ATTACHED TO FRU DEPENDS UPON WHICH SIO PORT THE FRU IS ASSIGNED (VIA ACU SERIAL COMMS DISPLAY ON OID). REFERENCE FIGURE 2.4.4 FOR SIO PORT-TO-PX RELATIONSHIP.
3. REFERENCE FIGURE 2.4.4 FOR PIN-TO-PIN WIRING BETWEEN SIO BOARDS W014/W016 DESTINATION CONNECTORS (PX).
4. SIGNAL DESCRIPTION
 TXD - TRANSMIT DATA
 RXD - RECEIVE DATA
 GND - GROUND



5202A18

Figure 2.4.10. Observer Notification Device and Peripheral Power

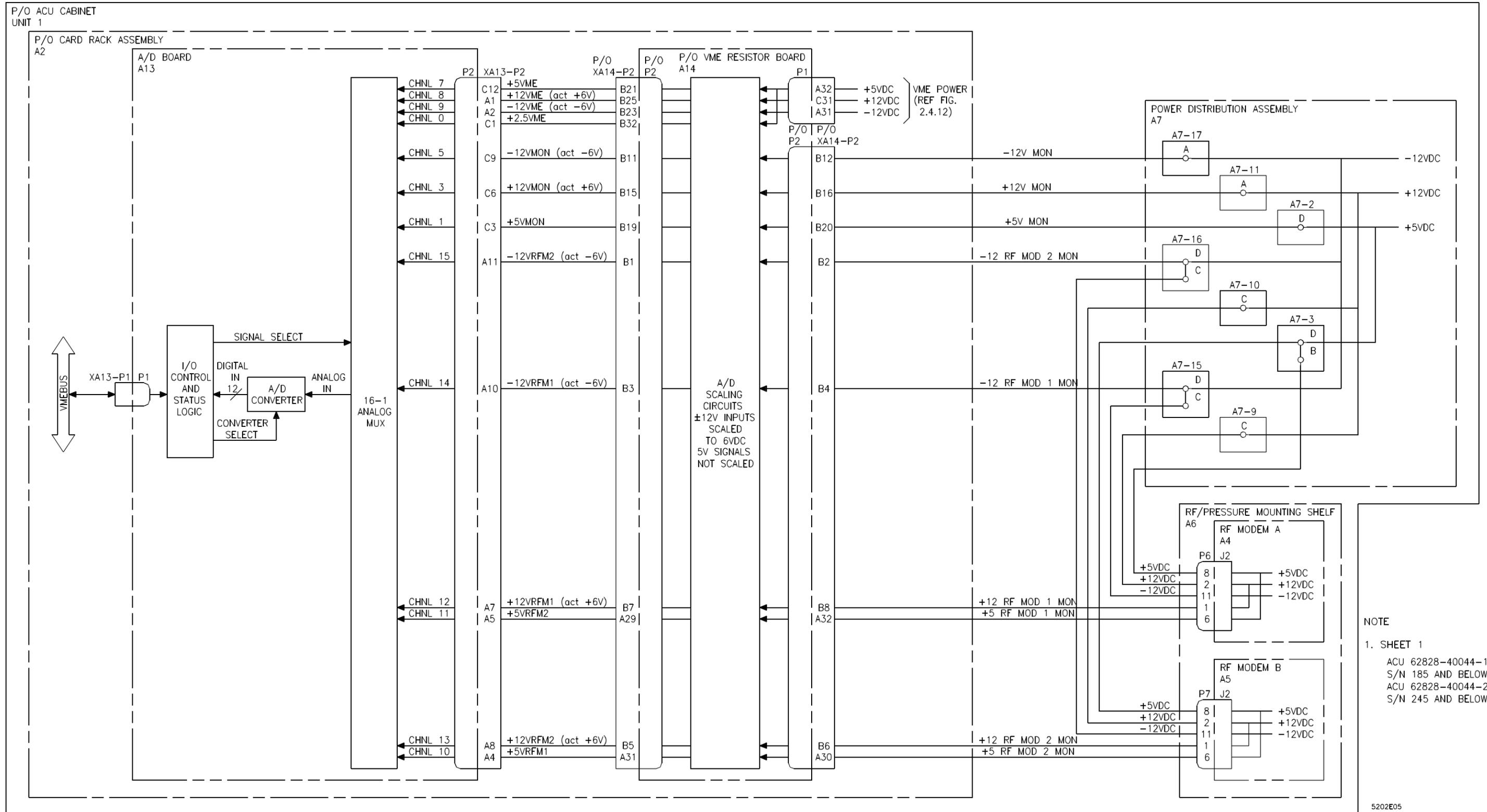


Figure 2.4.11. ACU Power and Signal Monitoring Detailed Block Diagram (Sheet 1 of 4)

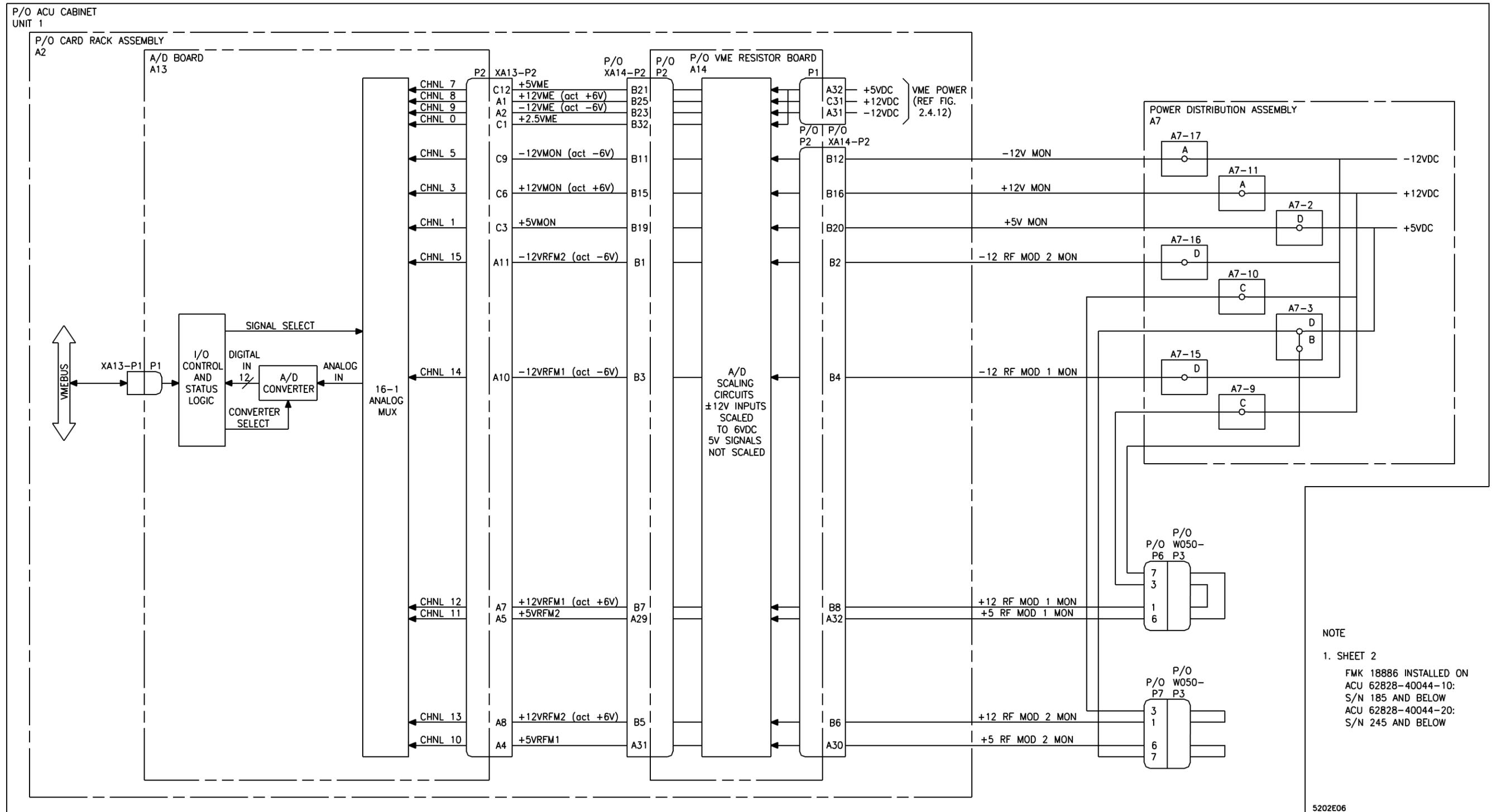


Figure 2.4.11. ACU Power and Signal Monitoring Detailed Block Diagram (Sheet 2)

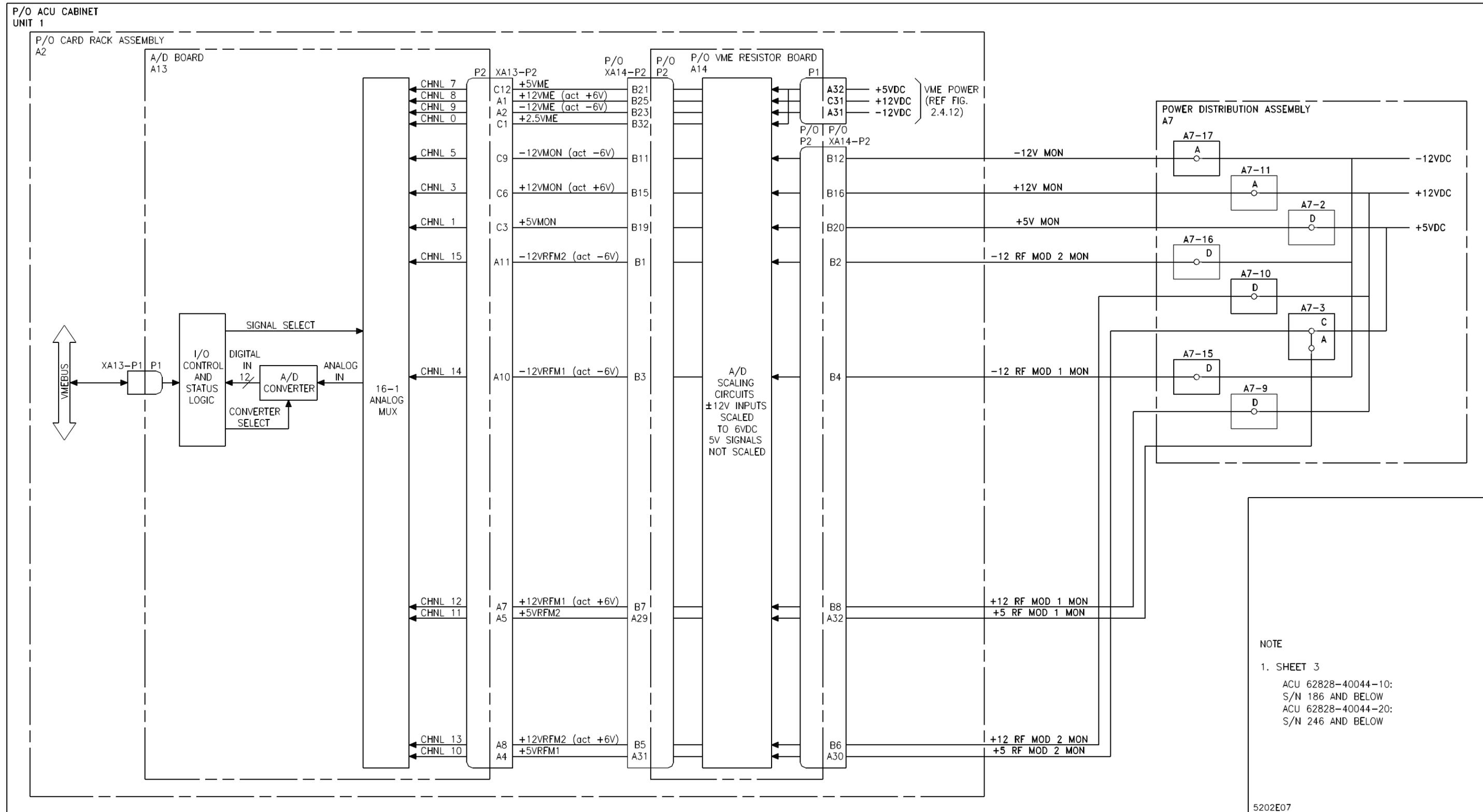


Figure 2.4.11. ACU Power and Signal Monitoring Detailed Block Diagram (Sheet 3)

The ACU power and signal monitoring circuitry consists of an A/D board, VME resistor board, and digital I/O board. The A/D board and DIO board each provide an interface to the VMEbus for access by the CPU (P1). These VMEbus interfaces contain control and status logic that identifies and conducts all VMEbus data transfers with the boards. The A/D board and DIO board also provide second interfaces for analog and digital user-defined devices (P2).

The A/D board contains 16 input analog channels numbered from 0 to 15 on the user interface port (P2). An analog multiplexer, under software control, selects 1 of the 16 possible analog signals for application to the A/D converter. The selected analog signal is converted to a 12-bit digital data value by the A/D converter that is then read by the computer over the VMEbus via the I/O control and status logic.

The analog input channels of the A/D board receive monitor signals corresponding to dc power supply outputs, rf modem power, and VMEbus (card rack assembly) power. All of these analog power signals are input via the VME resistor board. The VME resistor board scales ± 12 vdc power signals down to ± 6 vdc levels for the A/D converter. The 5 vdc power signals are passed through the VME resistor board unscaled. The voltages monitored at the actual power supply outputs are typically more than +5V and ± 12 V due to adjustments for losses between the power supplies and the loads.

The VME resistor board contains a precision voltage source that outputs a 2.5 ± 0.1 vdc reference voltage. This reference voltage is input on channel 0 of the A/D board. The CPU selects this signal for conversion during the ACU CST to test the operation of the A/D converter on the A/D board.

The digital I/O board allows the CPU to monitor the status of four digital status bits. These bits are the watchdog timer from the voice processor board, two status bits from the two dc power supplies, and UPS bypass status (Class II only). All signals except the UPS bypass status are routed through the VME resistor board before being applied to the digital I/O board. The power supply status bits (PS1/2GOOD) are normally at a logic 1 level. When a failure occurs in one of the power supplies, the corresponding status bit goes to logic 0. On the VME resistor board, a pulldown resistor is connected to each of the power supply status bits. The pulldown resistor ensures that the status bit goes to logic 0 to indicate a failure when the corresponding power supply is removed from the system. §
§
§

The ACU CST checks the status of the A/D board once per minute. The overall status of this board is displayed on the A/D page of the OID. The CST provides two tests for this board: REGISTER READBACK and REFERENCE VOLTAGE. The technician can manually run the A/D test from the A/D page at any time. A T status is displayed for all test categories until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The REGISTER READBACK test checks the ability of the CPU to write and read data to and from the board. The REFERENCE VOLTAGE test is based on the A/D board properly converting the 2.5 vdc reference voltage from the VME resistor board.

In addition to testing the A/D board, the CST also checks the status of each of the monitored power supply lines. The results of these checks are displayed on the ACU PWR page of the OID. The pass/fail status of all monitored 5 vdc and ± 12 vdc lines is displayed, along with the status of the 2.5 vdc reference voltage. Also given is the pass/fail indication for each of the two dc power supplies. The power supply checks are based on the status of the PSXGOOD bits input via the digital I/O board.

2.4.3.9 Power Distribution and Control. This paragraph contains detailed descriptions and detailed block diagrams of the ac/dc power distribution. The ACU is divided into two types of power distribution: ac and dc. The following paragraphs describe both the ac and dc power distribution.

2.4.3.9.1 **AC Distribution.** Class II ACU cabinets contain Power Supply Assembly 1A4, which provides UPS functions. Some Class I ACU's also contain a UPS as an option. Power Supply Assembly 1A4 can be one of two types, depending on the ACU serial number. The ACU's that have power supply assemblies installed are listed below with the effective serial numbers.

- a. Power supply assembly 62828-40124-10 is installed in ACU serial numbers 437 and below.
- b. Power supply assembly 62828-40265-10 is installed in ACU serial numbers 438 and above.

§ Power Distribution Assembly A7 provides the ACU with proper reset and UPS bypass capability. The
§ assembly consists of a solid state Time Delay Relay A7K1, Digital I/O Module A7K2 (Class II only), and
§ Power Relay A7K3 (Class II only). During initial turn-on, power is applied to solid state Time Delay Relay
§ A7K1 which delays power application for approximately three seconds then distributes power throughout
§ the ACU in Class I systems or applies power to Power Relay A7K3 normal closed contacts and Power
§ Supply Assembly A4. Power to Power Relay A7K3 normally closed contacts is routed through Power
§ Distribution Assembly A7 where it is distributed to the ACU assemblies.

§

§ After power is applied to Class II ACU assemblies, ASOS operational software monitors Power Relay A7K3
§ bypass status via Digital I/O Module A7K2 and Digital I/O Board A2XA15. When UPS status is good, Power
§ Relay A7K3 is energized via Digital I/O Board A1A2XA15 and Digital I/O Module A7K2 to route power from
§ the UPS output applied to Power Relay A7K3 normal open contacts to the ACU.

The following paragraphs describe ac power distribution for the two power supply assemblies.

2.4.3.9.2 **AC Distribution for Power Supply Assembly 62828-40124-10 (Figure 2.4.12).** Facility power is provided to the ACU via ACU INPUT POWER connector J41 on the I/O panel assembly. Input power is applied to Power Distribution Assembly 1A7 Power Reset Relay K1 which provides a three second delay to allow the pressure sensors and rf modems to stabilize after power is interrupted and then distributed throughout the ACU. For both Class I and Class II ACU's, blower B1 receives its ac power directly from the power distribution assembly.

For Class II systems (serial number 437 and below), a UPS is provided by Power Supply Assembly A4 and Battery Box A8 (serial number 437 and below). The UPS is not a unit in itself, but is the collection of the following eight units:

- a. Circuit breaker 1A4CB1
- b. 1.5 KVA Filter Board 1A4A3
- c. 1.5 KVA Inverter Board 1A4A4
- d. 1.5 KVA transformer 1A4T1
- e. Battery Box 1A8
- f. Fuse 1A4F1
- g. RS-232 Interface Board 1A4A2
- h. Status Panel Board 1A4A1

Input ac power is applied through circuit breaker CB1 to 1.5 KVA Filter Board A3. The filter board filters the input line voltage and routes it to 1.5 KVA Inverter Board A4 on the WHT/BLK (neut) and BLK/RED (line) wires of W030.

During normal (noninterrupted power) operation, the inverter board monitors the input voltage from the filter board and regulates it to provide a constant 120 vac output signal. The inverter board uses transformer T1 to perform this regulation. The secondary coil of T1 has multiple taps that are routed to tap-switching triacs on the inverter board. If the inverter board senses that the input line voltage is low, it causes one of the triacs to switch in a T1 secondary tap that steps up the voltage to the required level. The stepped-up voltage is then output from the BLK/WHT terminal of the inverter board to connector S10 of 1.5 KVA Filter Board A3. Similarly, if the inverter board senses that the input ac voltage is high, the T1 secondary tap is changed to step the voltage down to the required level, and the stepped-down voltage is output to the filter board. The filter board filters the ac voltage and outputs the regulated voltage from connector J7 as the UPS ac output signal.

When the inverter board senses a loss of its input ac signal, it uses transformer T1 to convert dc voltage from Battery Box A8 to a backup ac signal. Battery Box A8 contains five 12 vdc batteries wired in series to provide a total of 60 vdc. This dc voltage is applied through fuse F1 to the RED terminal of the inverter board, where it is then routed to the center tap of the primary coil of T1. When the inverter board senses a loss in the input ac signal from the inverter board, it alternately switches in the two other two primary leads of T1 (BLU2 and YEL2). This causes alternating current in the T1 primary, which is induced to the secondary coil of T1. The inverter board then uses its tap-switching triacs, as described above, to output a regulated ac voltage to the filter board.

The regulated, filtered UPS ac output signal from the filter board is routed to Power Distribution Assembly A7 for distribution to ACU assemblies. Units that receive the UPS output voltage from the power distribution assembly are the dc power supply enclosure, the card rack assembly, and the modem ac power rack. UPS ac voltage is also routed to PERIPHERAL POWER connector J40 on the I/O panel assembly to provide backed up ac power to the primary OID, the printer, and to FAA modems.

RS-232 Interface Board A2 allows the CPU to monitor the operational status of the UPS. The inverter board contains circuitry to monitor the status of the ac input and output voltages, battery voltages, tap-switching triac status, etc. During CST, the CPU communicates with the inverter board, via the RS-232 interface board, to obtain these status data. The CPU analyzes these UPS data and displays the results on the ACU UPS page of the OID.

The ACU CST checks the status of the UPS once per minute. CST results are displayed on the ACU UPS page of the OID. The CST performs 10 tests on the UPS. These tests are based on information determined by the 1.5 KVA inverter board and communicated to the CPU via the RS-232 interface board. The technician can manually run the UPS test from the UPS page at any time. A T is displayed for the 10 test categories until the test is run again during the next CST cycle. After the cycle, the latest test status is displayed and the fail count (if applicable) is incremented.

The BATTERY VOLTAGE test indicates the current voltage provided by the battery box. The INPUT VOLTAGE test indicates the current value (in vac) of the facility input voltage being received by the inverter board from the 1.5 KVA filter board. The OUTPUT VOLTAGE test indicates the current value (in vac) of the regulated ac voltage being output from the inverter board to the filter board. The OUTPUT ENABLED test indicates whether or not the UPS output is currently enabled or disabled via the OUTPUT POWER switch on the status panel. The ON AC LINE test indicates the power source on which the UPS is operating (P = facility input (ac line), F = UPS operating on battery backup). The BATTERY STATUS test indicates the condition of the battery box supply. The TRIAC STATUS test indicates the operating condition of the tap changing triacs on the inverter board. The TEMPERATURE test checks for an overheat condition as detected by a sensor on the inverter board. The RS-232 test checks for transmission errors encountered by

the RS-232 interface board. Finally, the TIMEOUT test indicates a failure in the event that the CPU receives no response at all from the RS-232 interface board.

In a Class I ACU that does not contain a UPS (UPS is an option in a Class I ACU), jumpers are installed between the UPS input and UPS output terminals on Power Distribution Assembly 1A7. That is, wires are installed between terminals A7-18C and -23A (115 vac), and between terminals -19C and -22C (neutral) to bypass the Class II UPS described above.

2.4.3.9.3 AC Distribution for Power Supply Assembly 62828-40265-10 (Figure 2.4.13). Facility power is provided to the ACU via ACU INPUT POWER connector J41 on the I/O panel assembly. Input power is applied to Power Distribution Assembly 1A7 for distribution throughout the ACU. For both Class I and Class II ACU's, blower B1 receives its ac power directly from the power distribution assembly. For Class II systems (serial number 438 and above), facility power is provided by Power Supply Assembly 1A4 and Battery Box 1A8.

Input ac power is applied through connector P97. During normal (noninterrupted power) operation, the UPS assembly monitors the input signal internally and maintains a steady output voltage.

When the UPS detects a loss in its input ac voltage, it inverts dc voltage from Battery Box 1A8 to a backup ac voltage. Battery Box 1A8 contains four 12-vdc batteries wired in series to provide a total of 48 vdc.

The regulated, filtered UPS ac output signal from the UPS is routed to Power Distribution Assembly 1A7 for distribution to ACU assemblies. The dc power supply enclosure and the modem ac power rack receive the UPS output voltage from the power distribution assembly. UPS ac voltage is also routed to PERIPHERAL POWER connector J40 on the I/O panel assembly to provide backed-up ac power to the primary OID, the printer, and FAA modems. An UPS bypass circuit has been added to Class II ACU's, which allows the ACU to operate from unconditioned ac power input in the event that the UPS fails or is undergoing maintenance. The bypass circuit includes three relays. A 1-second time-delay relay, A7K1, ensures that whenever primary power is interrupted briefly, it cannot be reapplied for 1 second, so that power-up reset circuits in ACU FRU's will correctly reset those FRU's. Solid-state relay A7K2 allows software control of the UPS bypass function; software control can be disabled by jumpering terminals 1 and 2. A7K2 normally connects the coil of ac power relay A7K3, a triple-pole, double-throw relay, to UPS output, so that it will be energized whenever UPS is providing an output. When the software command is active, A7K2 contacts open to release A7K3, bypassing the UPS and connecting the unconditioned primary ac power input to ac power distribution. The third set of A7K3 contacts, when the relay is released, sends a ground signal to the DIO board to indicate that unconditioned primary input power is selected.

The RS-232 COMM PORT on the UPS allows the CPU to monitor the operational status of the UPS. The UPS contains circuitry to monitor the status of the ac input and output voltages, battery voltages, etc. During CST, the CPU communicates with the UPS to obtain these status data. The CPU analyzes these UPS data and displays the results on the ACU UPS page of the OID.

The ACU polls the UPS approximately every 2 minutes with a dump status command to obtain a current status of the UPS. BATTERY VOLTAGE status (provided as a numerical value) indicates the current voltages provided by the battery box. INPUT VOLTAGE status (provided as a numerical value) indicates the current value (in vac) of the facility input voltage being received by the UPS. OUTPUT VOLTAGE status (provided as a numerical value) indicates the current value (in vac) of the regulated ac voltage being output from the UPS. UPS OPERATION status indicates whether or not the UPS is functioning in a normal (indicated by a P (utility is OK, battery is OK, and UPS is in its normal state)) or abnormal operation (indicated by an F). The ON AC LINE status indicates the power source on which the UPS is operating

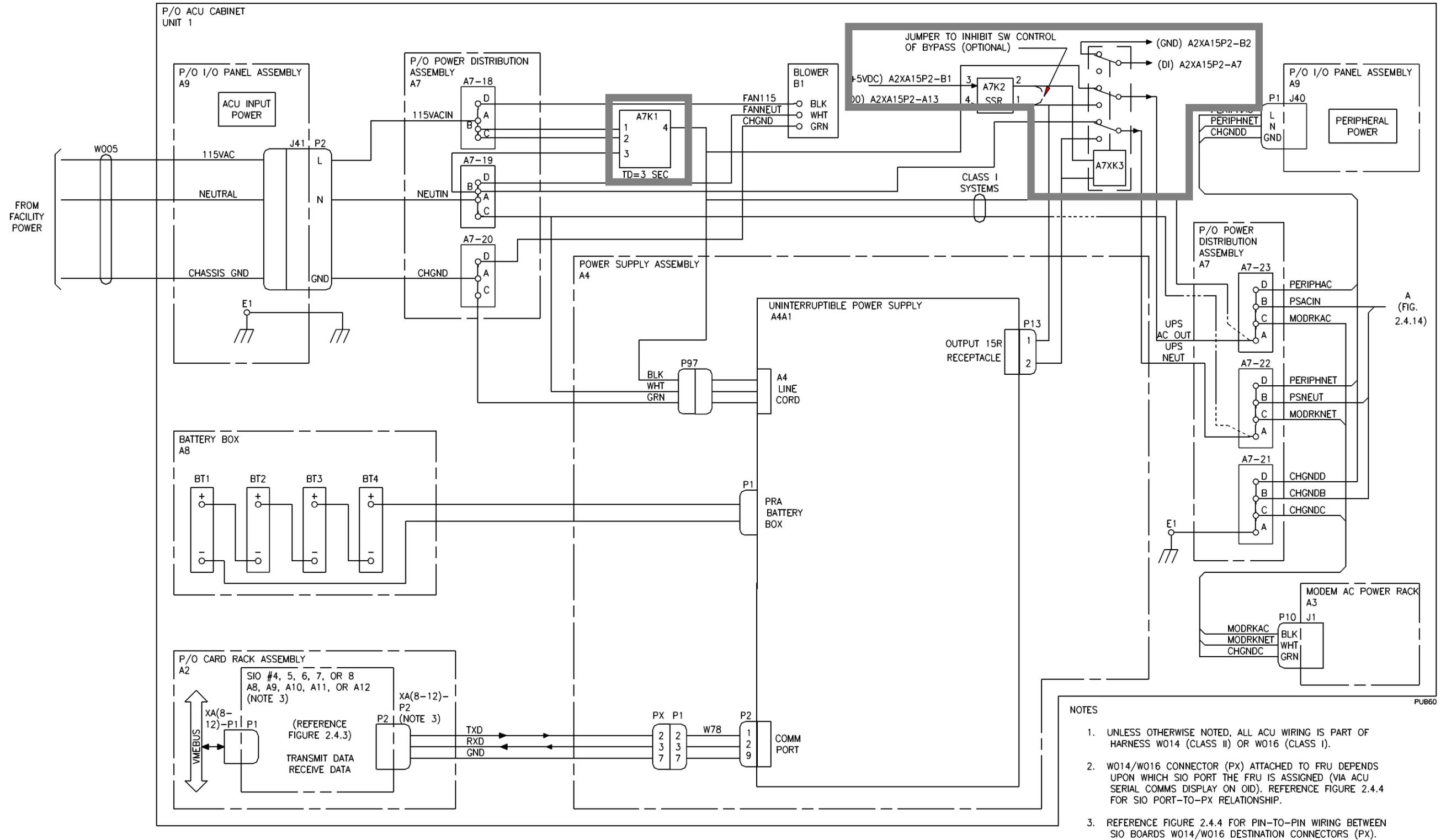


Figure 2.4.13. ACU AC Power Distribution Detailed Block Diagram for 62828-40265-10

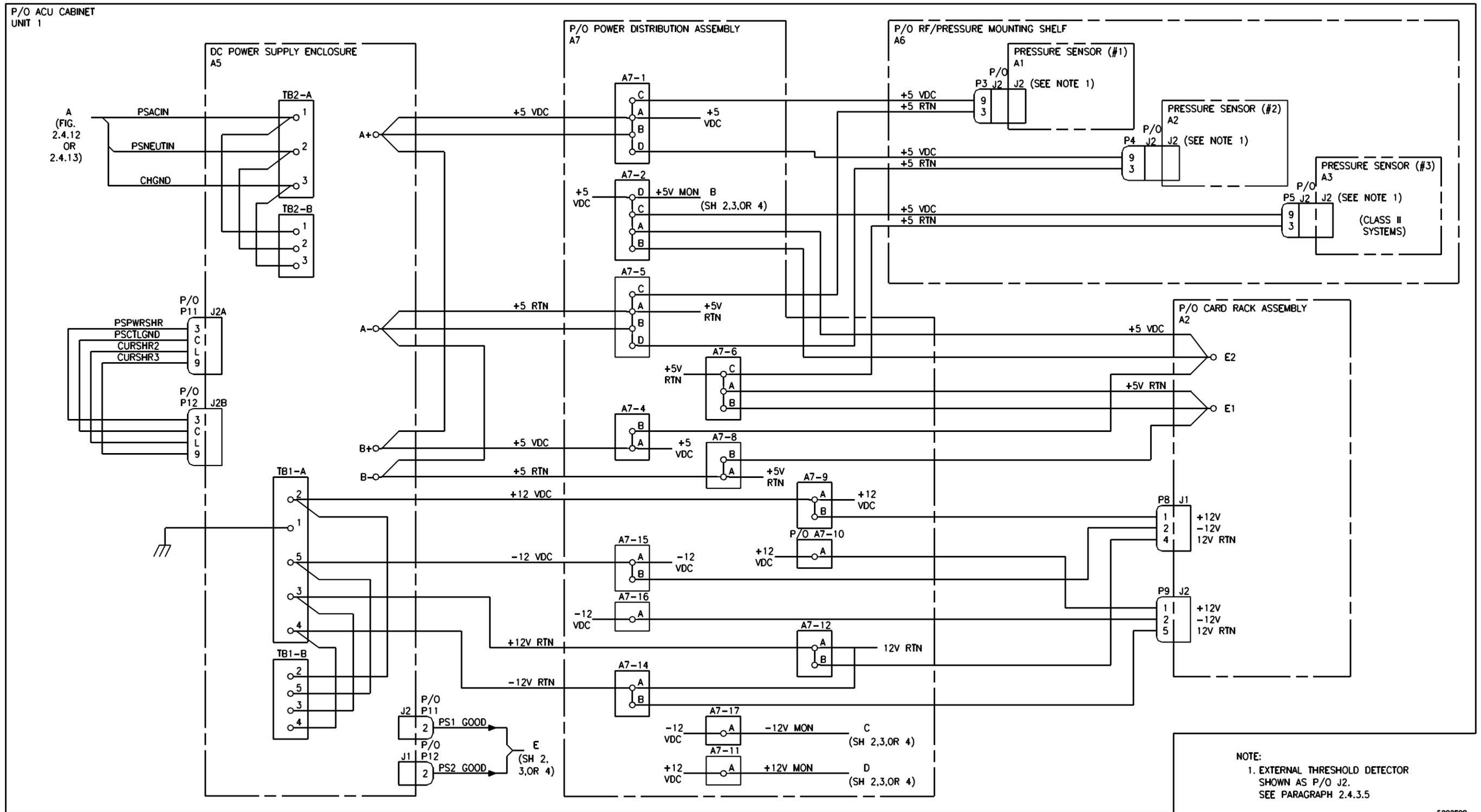
(P = facility input (ac line), F = UPS operating on battery backup). BATTERY STATUS (P for pass or F for fail) indicates whether battery power is low from the battery box supply. INVERTER status indicates whether the internal inverter is operating in overvoltage or undervoltage status. GROUND STATUS (P for pass or F for fail) checks for a ground failure. UTILITY status (P for pass or F for fail) indicates an overvoltage or unsynchronized signal from facility power. TIMEOUT status (P for pass or F for fail) indicates a failure in the event that the CPU receives no response at all from the UPS. BATTERY MANAGEMENT status (provided as a word description) indicates if the current from the batteries is FLOATING (trickle charge), RESTING (not charging or discharging), CHARGING, or DISCHARGING. Finally, LINE REGULATION status (provided as a word description) indicates if the UPS is maintaining a STEP-UP, STEP DOWN, or NORMAL voltage from facility power.

In a Class I ACU without a UPS (UPS is an option in a Class I ACU), jumpers are installed between the UPS input and output terminals on Power Distribution Assembly 1A7; that is, wires are installed between terminals -18C and -23A (115 vac) and between terminals -19C and -22C (neutral) to bypass the Class II UPS described above.

2.4.3.9.4 **DC Power Distribution.** Figure 2.4.14, sheets 1 through 6, illustrate dc power distribution. Sheet 1 shows the common dc circuitry for all rf modem installations. Sheets 2 through 6 show five different configurations of dc power distribution wiring, depending on the rf modem installation (paragraph 2.4.3.4.2) as follows:

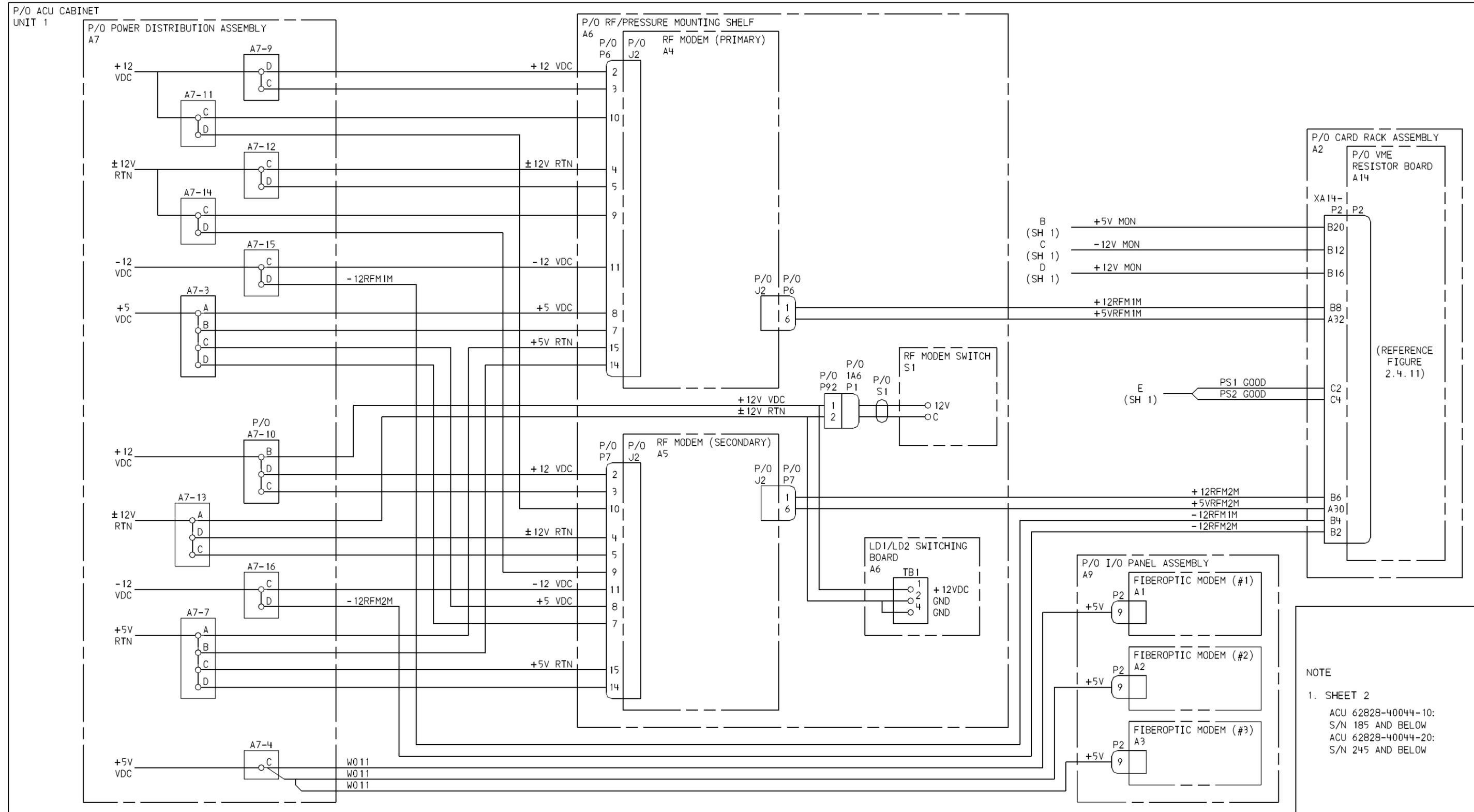
- Sheet 2- original equipment AAI rf modem configuration
- Sheet 3- as sheet 2 but shown modified for Motorola rf modems
- Sheet 4- as sheet 3 but shown with Johnson Data modems
- Sheet 5- original equipment Motorola rf modem configuration
- Sheet 6- as sheet 5 but shown with Johnson Data modems

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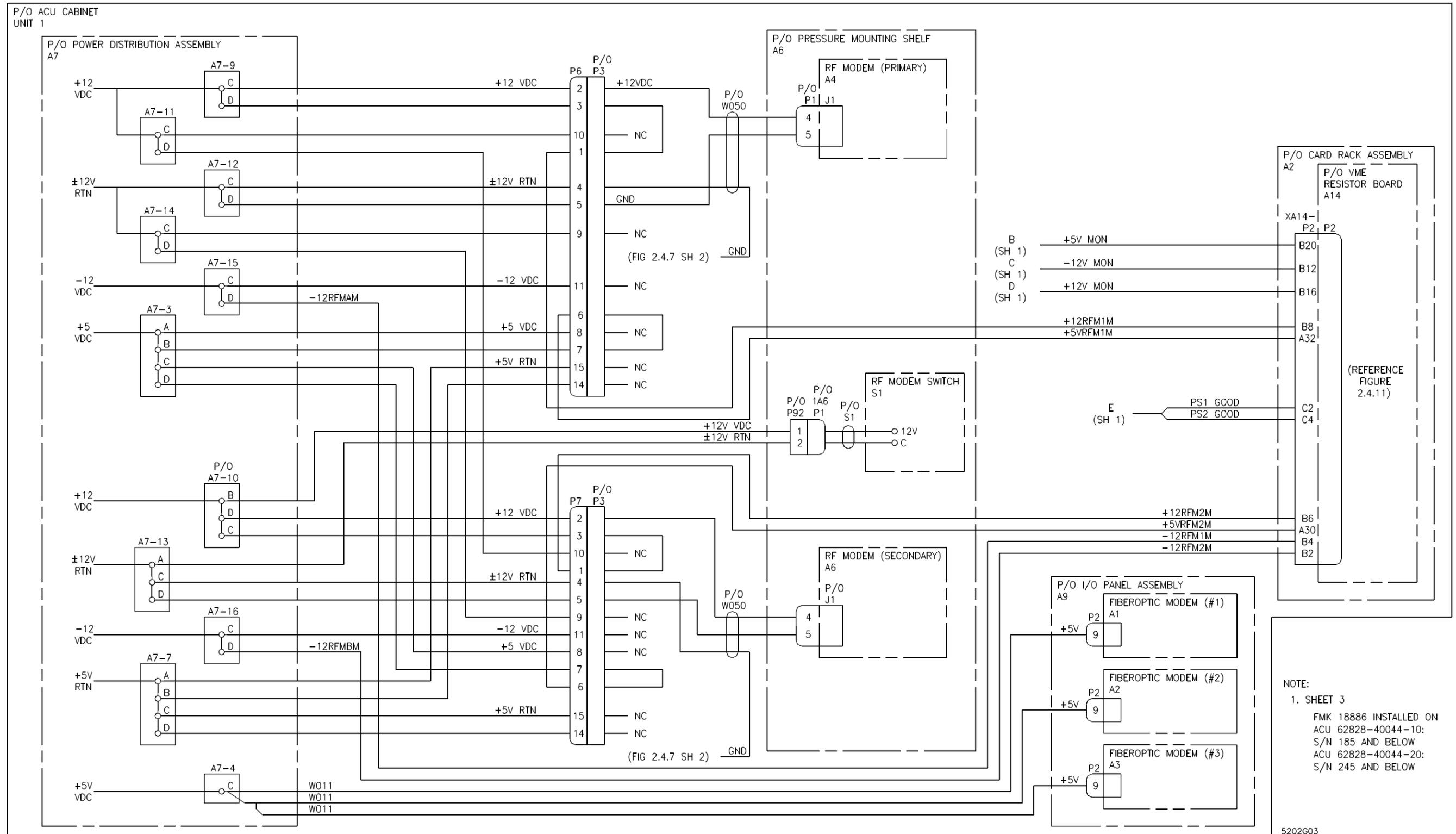
5202F08

Figure 2.4.14. ACU DC Power Distribution Detailed Block Diagram (Sheet 1 of 6)



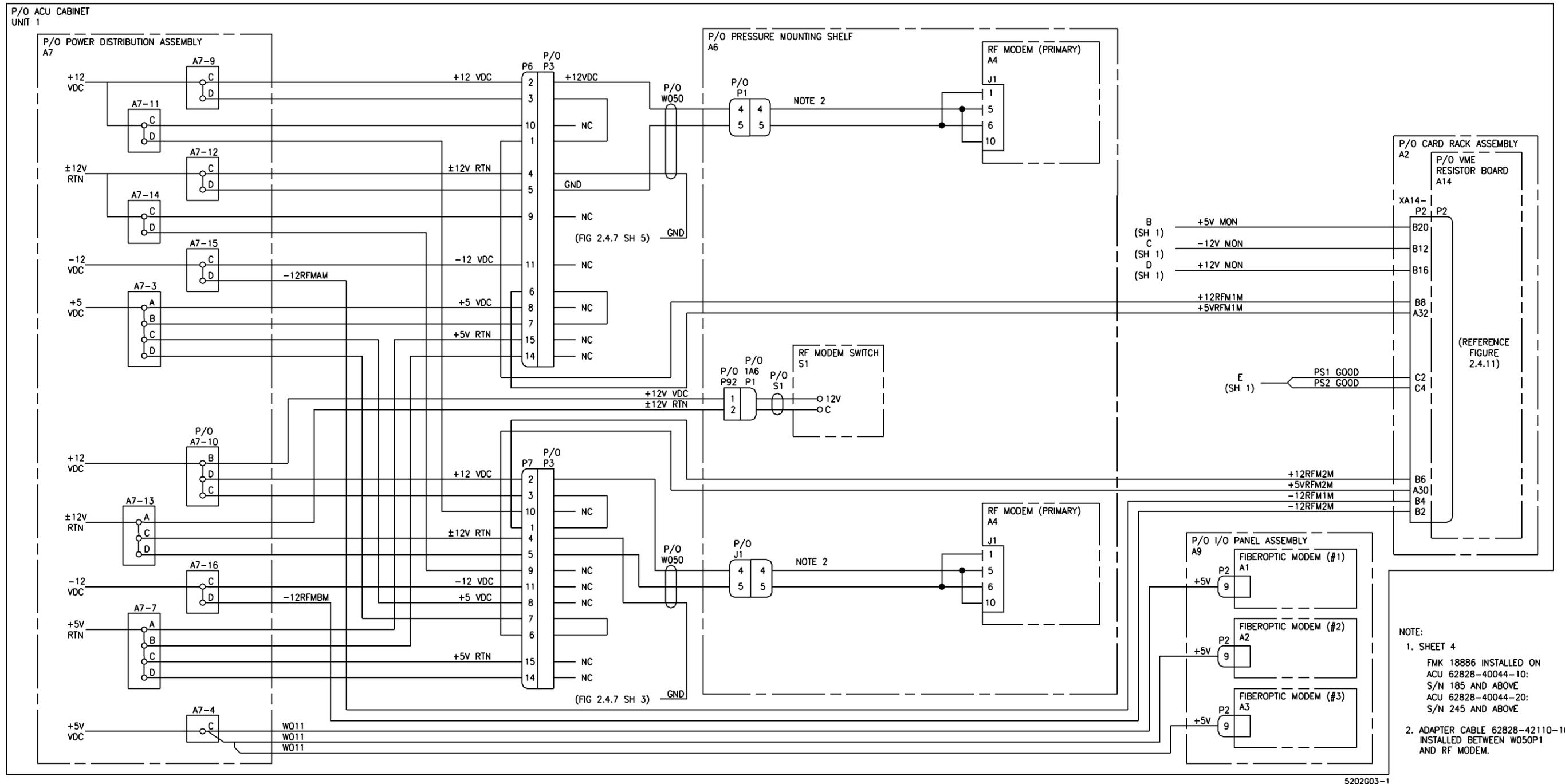
AAI MODEMS

Figure 2.4.14. ACU DC Power Distribution S
Detailed Block Diagram (Sheet 2 of 6)



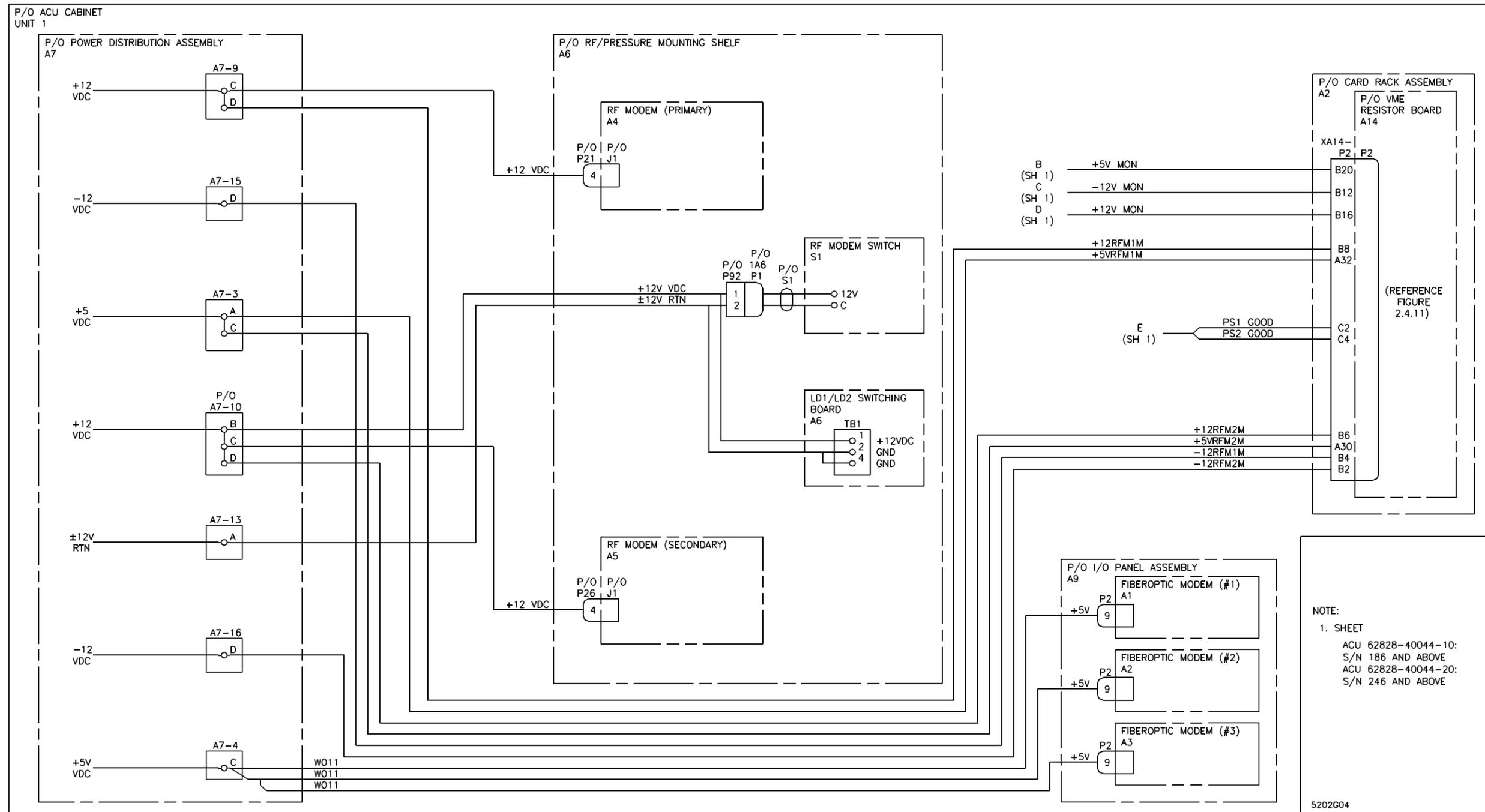
SYSTEM CONVERTED FROM AAI
MODEMS TO MOTOROLA MODEMS

Figure 2.4.14. ACU DC Power Distribution
Detailed Block Diagram (Sheet 3 of 6)



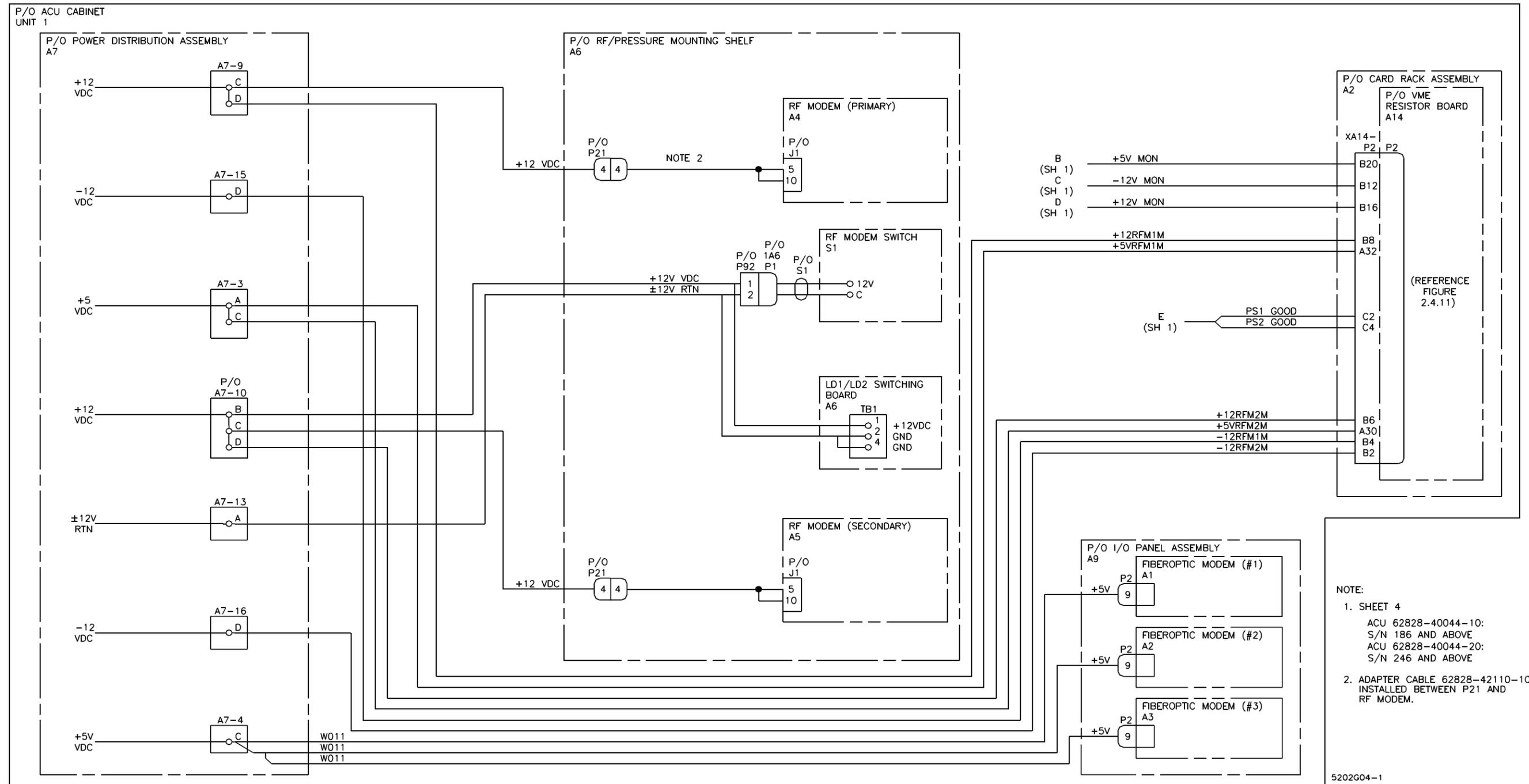
**SYSTEM CONVERTED FROM AAI MODEMS TO MODEMS
EQUIPPED WITH JOHNSON DATA MODEMS**

**Figure 2.4.14. ACU DC Power Distribution
Detailed Block Diagram (Sheet 4 of 6)**



MOTOROLA MODEMS

Figure 2.4.14. ACU DC Power Distribution Detailed Block Diagram (Sheet 5 of 6)



SYSTEM CONVERTED FROM MOTOROLA
MODEMS TO JOHNSON DATA MODEMS

Figure 2.4.14. ACU DC Power Distribution
Detailed Block Diagram (Sheet 6 of 6)

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